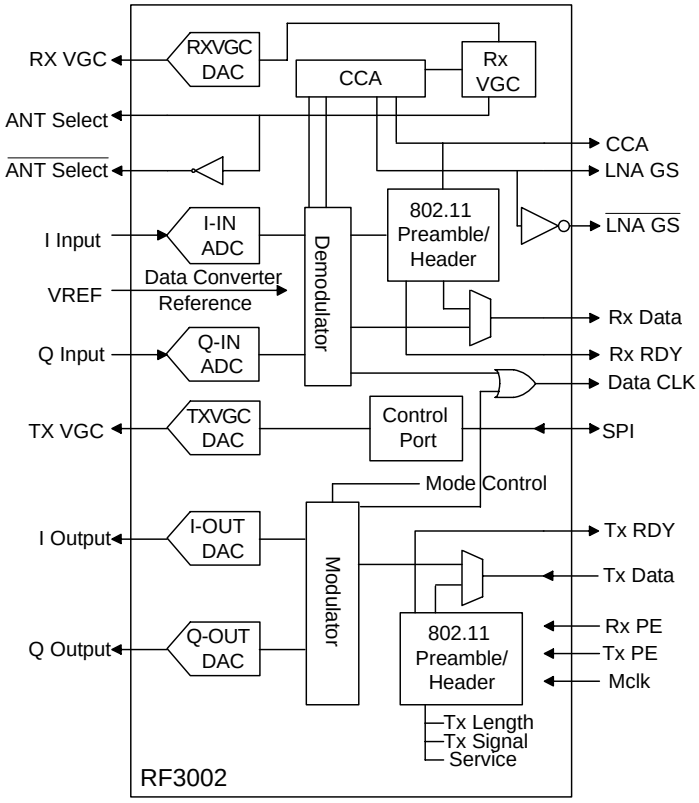
RoHS Compliant & Pb-Free Product

Features

- On-Chip ADCs and DACs, RSSI, AGC
- BPSK/QPSK/CCK
- 250nS Delay Spread Equalizer
- Supports Antenna Diversity
- Reference Design Available

Applications

- IEEE802.11b WLAN Systems
- ISM Band Systems
- Direct Sequence Systems
- Wireless Modems
- Wireless Point-to-Point



Functional Block Diagram

Product Description

The RF3002 is a complete spread-spectrum baseband processor, utilizing PSK and CCK modulation. It is suitable for use in 11Mbps IEEE 802.11b wireless LAN systems. The RF3002 performs all of the functions necessary to modulate a digital data source for transmission in a wireless environment.

In IEEE 802.11b operation, the RF3002 will manage preamble and header generation and extraction. The RF3002 expects raw packet data at the transmit data port, and will provide the same at the receive data port. The RF3002 includes an on-chip equalizer to provide protection against multi-path events while operating in high data rate modes.

The architecture of the RF3002 allows the host processor to easily reconfigure parameters via a four-wire SPI port.

A complete 2.4GHz radio reference design is also available from RF Micro Devices.

Optimum Technology Matching® Applied

☐ Si BJT	☐ GaAs HBT	☐ GaAs MESFET
☐ Si Bi-CMOS	☐ SiGe HBT	☑ Si CMOS
☐ GaInP/HBT	☐ GaN HEMT	☐ SiGe Bi-CMOS

Ordering Information

RF3002	Spread-Spectrum Baseband Modem
RF3002PCBA-41X	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	+4.0	V_{DC}
Input, Output or I/O Voltage	Ground-0.5 to VCC+0.5	V_{DC}
Voltage	2.7 to 3.6	V
VDDD Output	2.7	V_{DC}
Max. Storage Temperature	-65 to +150	°C
Max. Junction Temperature	+150	°C
Operating Ambient Temperature	-40 to +85	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Electrical					See Figures 15 and 16. V_{CC}=3.0V to 3.3V±10%, T_Z=-40°C to +85°C
Power Supply Voltage	2.7	3.3	3.6	V	VDDA
		2.2		V	VDDD, Output Only.
V_{REF}	1.6	1.7	1.8	V	No current draw.
Input Voltage	V_{DDA}-0.2	V_{DDA}	V_{DDA}+0.2	V	Logical "1" (V_{IH})
	-0.2	0	+0.2	V	Logical "0" (V_{IL})
Output Voltage		V_{DDA}-1.0		V	Logical "1" (V_{OH})
		0.2	0.7	V	Logical "0" (V_{OL})
Current Consumption		25		mA	Transmit Mode (I_{TX})
		50		mA	Receive Mode (I_{RX})
Sleep Mode		0.7	1.0	mA	Mode 1, Reset Active, No Clocks (I_{S1})
		1.3	1.5	mA	Mode 2, Reset Inactive, No Clocks (I_{S2})
Input Leakage Current			10	µA	I_I
Output Leakage Current			10	µA	I_O
Output Loading		20	20	pF	
AC Electrical					V_{CC}=3.0V to 3.3V±10%, T_A=-40°C to +85°C. See Note 1.
M CLK Duty Cycle	40/60		60/40	%	
Rise/Fall	-		10	nS	All outputs. See Notes 2 and 3.
TXPE to I_{OUT}/Q_{OUT}			3.1	µS	1st valid chip. 802.11 modes.
TXDATA to I/Q_{OUT}			1.0	µS	
TXPE Inactive Width	1			µS	See Notes 2 and 4.
TXRDY Active to 1st DATACLK Hi	500			nS	
Setup TXDATA to DATACLK	10			nS	
Hold TXDATA to DATACLK Hi	10			nS	
Reset to TXPE	100			µS	
Reset to RXPE	100			µS	
TXDATA Modulation Extension	2			µS	See Notes 2 and 5.
RXPE Inactive Width	0			nS	See Notes 2 and 6.
DATACLK Period	68			nS	11 Mbps Mode
DATACLK Width Hi or Low	15	44	68	nS	11 Mbps Mode
DATACLK to RX Data	30			nS	
RXRDY to 1st DATACLK	40			nS	See Note 2.
RXDATA to 1st DATACLK	40			nS	
Setup RXDATA to DATACLK	30			nS	
RESET Width Active	40			nS	See Note 2.
CCA Valid			15	µS	See Note 2, RX Packet to CCA.
RXPE to RSSI Valid			15	µS	See Note 8.
I/Q_{IN} to RXDATA			2.25	µS	

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
I/Q ADC					
Full Scale Input Voltage		0.7	+10%	V_{P-P}	See Note 7.
Input Bandwidth		11		MHz	
Input Capacitance		5		pF	
Input Resistance	50			kΩ	
I/Q DAC					
Full Scale Output Voltage		200		mV	See Note 7.
Sample Rate		11		MHz	
Resolution		6		bits	
DNL		0.5		LSB	
INL		0.5		LSB	Tested for monotonicity.
TX VGC DAC					
Maximum Gain Output Voltage		1.2		V	
Minimum Gain Output Voltage		2.0		V	
Resolution		6		bits	
DNL		0.5		LSB	
INL		0.5		LSB	
RX VGC DAC					
Maximum Gain Output Voltage		1.2		V	
Minimum Gain Output Voltage		2.0		V	
Resolution		6		bits	
DNL		0.5		LSB	
INL		0.5		LSB	Tested for monotonicity.
Control Port Timing Characteristics					
SPI Mode					Mode Switching Characteristics. See Figure 3.
C CLK Clock Frequency			6	MHz	f_{CLK}
CS High Time Between Transmissions	1.1			μS	t_{CSH}
CS Falling to C CLK Edge	22			nS	t_{CSS}
C CLK Low Time	68			nS	t_{CLKL}
C CLK High Time	68			nS	t_{CLKH}
CD IN to C CLK Setup Time	42			nS	t_{DSU}
C CLK Rising to Data Hold Time	16			nS	t_{DHLD}
C CLK Falling to CD OUT Stable			47	nS	t_{PD}

Notes:

1. AC tests performed with C_L=20pF, I_{OL}=2mA, and I_{OH}=-1mA. Input reference level all inputs V_{CC}/2. Test V_{IH}=V_{CC}, V_{IL}=0V; V_{OH}=V_{OL}=V_{CC}/2.
2. Not tested, but characterized at initial design and at major process/design changes.
3. Measured from V_{IL} to V_{IH}.
4. TX PE must be inactive before going active to generate a new packet.
5. I_{OUT}/Q_{OUT} are modulated after last chip of valid data to provide ramp-down time for RF/IF circuits.
6. A new search will begin after last bit of 802.11 packet in 802.11 modes.
7. Centered about 1.7V V_{REF}.
8. Accurate to within ±3dB of final gain setting.

For more information on Figure 1, see parameter table (on previous pages).

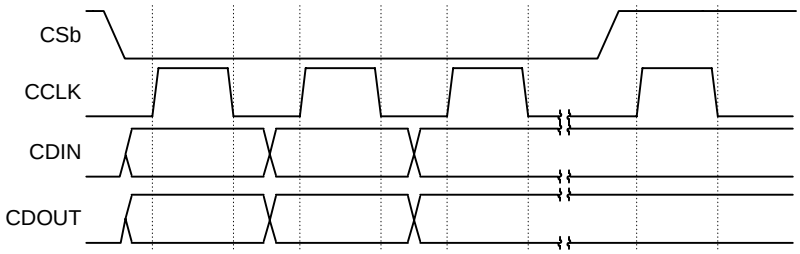


Figure 1. SPI Timing Transition Detail

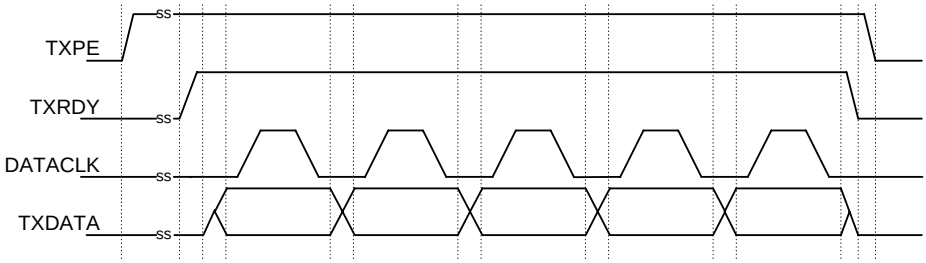


Figure 2. Transmit Port Detail Timing

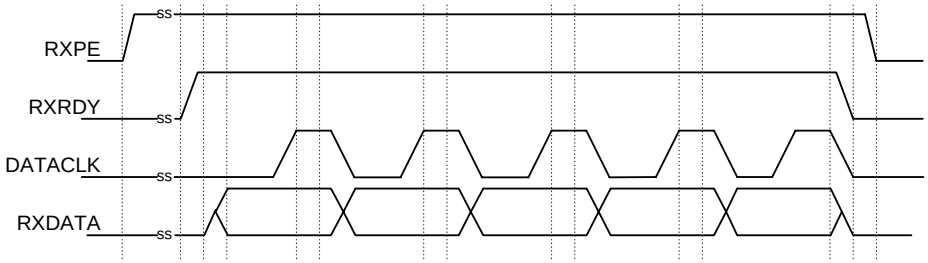
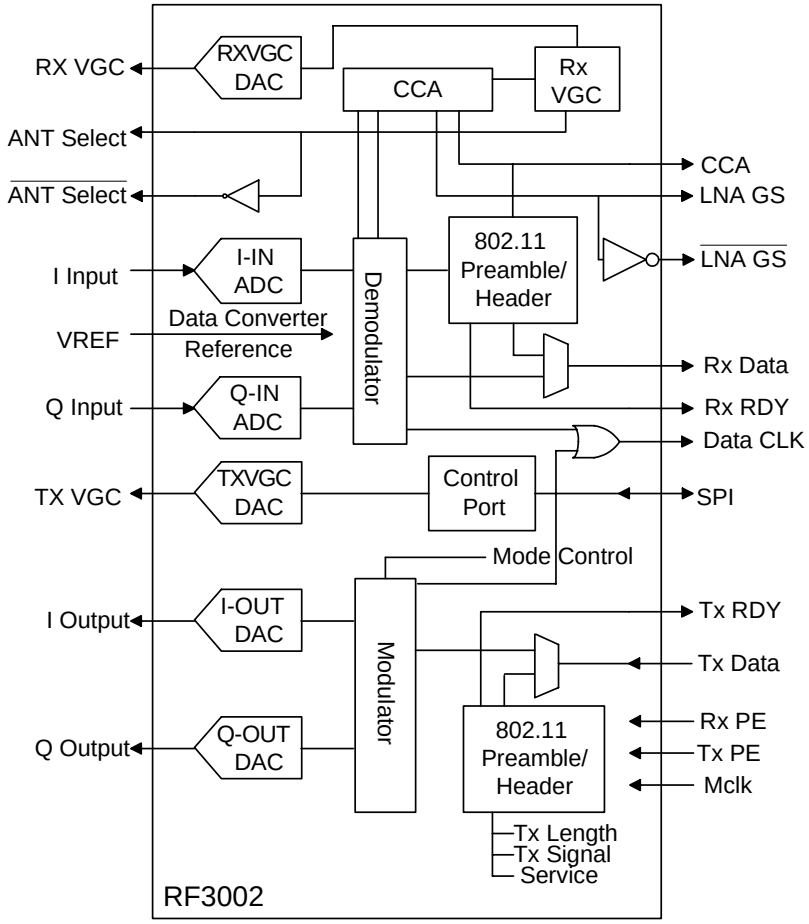


Figure 3. Receiver Port Detail Timing

Index

Pin	Function	I/O Type	Description
1	DATACLK	O	Data clock for TX and RX data.
2	RXDATA	O	RX data stream output.
3	CSb	I	In SPI mode this pin serves as serial port chip select.
4	CCLK	I	Serial port clock. This clock is used for SPI mode.
5	CDIN	I	In SPI mode this pin serves as CDIN input.
6	CDOUT	O	In SPI mode this pin serves as CDOUT output.
7	RXVGC	O	Analog receive variable gain control output: 1.2V to 2.0V.
8	NC	NC	Not connected.
9	NC	NC	Not connected.
10	IIN	I	Analog I input.
11	QIN	I	Analog Q input.
12	VDDA	POWER	DC power for analog sections 3.3V.
13	GNDA	GROUND	Ground signal for analog power.
14	IOUT	O	Analog I output: 1.6V to 1.8V.
15	QOUT	O	Analog Q output: 1.6V to 1.8V.
16	TXVGC	O	Analog voltage for transmitter variable gain control: 1.2V to 2.0V.
17	ANTSELB	O	
18	ANTSEL	O	Antenna selection signal for diversity receiver.
19	RESET	I	Pin='1' chip reset. Pin='0' standard operation.
20	VREF	I	Reference voltage for internal data converters. Connect to RF2948 V_{REF} or set to 1.7V_{DC}.
21	TXPE	I	Input from the external network processor. The rising edge of TX PE places the transmitter into an active state. The falling edge of TX PE indicates the end of transmission.
22	RXPE	I	When active (value '1'), the receiver is powered up and CCA circuitry is active.
23	MCLK	I	Master clock. This should be a 44MHz for IEEE802.11b and is used to generate other internally used clocks.
24	NC	NC	Not connected.
25	TXRDY	O	Indicates that the chip is ready to accept data from the MAC for Tx.
26	RXRDY	O	Indicates that the chip is ready to deliver data to the MAC from Rx.
27	VDDD	NC	Output from 2.2V internal voltage regulator for digital sections of RF3002. This pin should not be connected to anything.
28	GNDD	GROUND	Ground signal for digital power.
29	CCA	O	Clear channel assessment per IEEE802.11b standard. “1” indicates “clear”.
30	LNAGSB	O	
31	LNAGS	O	LNA gain select. “1” indicates “high gain”.
32	TXDATA	I	TX data stream input.

Detailed Functional Block Diagram



General Description

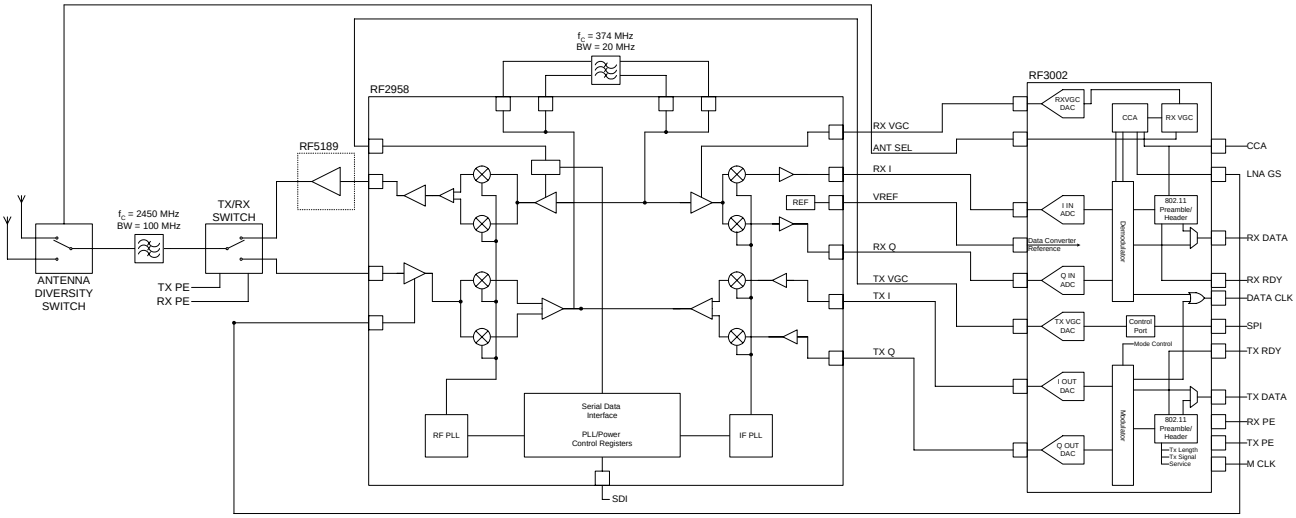


Figure 4. 2.4GHz IEEE802.11b Chipset Diagram

Figure 4 shows the complete 2.4GHz chipset, and where the RF3002 fits into the system. The RF3002 is a complete spread-spectrum transceiver, allowing PSK system operation. The RF3002 performs all of the functions necessary to modulate a digital data source for transmission in a wireless environment. When operating in IEEE802.11b modes, the RF3002: handles preamble and header generation and extraction; automatic gain control; clear channel assessment; antenna diversity; and, implements an equalizer to handle multi-path events at high data rates.

SPI Control Port

The control port is used by the Media Access Controller (MAC) to set up and modify the multiple operation modes of the RF3002. The port is set to SPI mode, with the RF3002 acting as Slave. Note that if no setup information is programmed into the RF3002's registers, it will default to a BPSK 1Mbps IEEE802.11b DSSS mode. If an IEEE802.11b mode is selected in Register 1, other waveform registers are ignored and the appropriate, standards compliant features are enabled (e.g., PN code, preamble/header, etc.). TX length is required for all IEEE802.11b modes.

All Registers, as defined in the Register Definition section of this datasheet, can be read in real time through this control port. Selected registers, as indicated in the Register section are read-only.

The control port of the RF3002 contains a mode to automatically increment the register pointer, allowing reading or writing of adjacent bytes without the need to stop and restart control port access.

SPI Mode Description

SPI mode pin definitions.

Pin Name	Description
$\overline{CS}$	Serial port chip select. A value of '0' is port enabled.
C CLK	Control port-bit clock input from serial port master.
CD IN	Serial data input to the RF3002. Data is clocked in on the rising edge of C CLK.
CD OUT	Serial data output from the RF3002. Data is clocked out on the falling edge of C CLK.

SPI Method of Operation

Write:

To Write into a register of the RF3002, the accessing SPI master needs to simply bring $\overline{CS}$ low, then Address the RF3002 (0100000_2) and provide a '0' for the Read/Write-bit. The user should note that all data transfers to/from the RF3002 are msb first. This should be followed by the Auto-increment-bit and the Memory address pointer (MAP), this is an 7-bit value to indicate the initial address for the write process. Register data is to immediately follow the MAP. If the Auto-Increment-bit is set RF3002 will continue to write data 1 byte at a time into the address pointed to by the MAP, and increment the MAP after each byte. When the SPI Master is finished filling registers, it must raise $\overline{CS}$ to indicate the cycle end.

Read:

Reading the contents of the RF3002 internal registers, the procedure is actually a write process followed by the read. The SPI Master must bring $\overline{CS}$ low, to prepare the RF3002 to look for its address. The SPI Master now addresses the RF3002, by placing the RF3002 base address (0100000_2) on the data bus and append a '0' for the Read/Write-bit. The SPI Master must now set the Auto-increment-bit and initialize the 7-bit MAP to the value of the register to be read. The user should raise $\overline{CS}$, to end the write portion of the cycle. To complete the Write/Read cycle the SPI Master now needs to lower $\overline{CS}$ again, and readdress the RF3002 providing a '1' for the Read/Write-bit. Once this is completed the RF3002 will begin outputting the register contents. As long as the $\overline{CS}$ remains low, and the auto-increment bit is set, the RF3002 will auto-increment the MAP. When the RF3002 reaches Address 31, the MAP will be reset to Register 0 and the process continues.

SPI Operation Summary

To Write:

1. Bring $\overline{CS}$ low.
2. Chip Address (7-bits) - This should match the RF3002 chip address of 0100000_2.
3. Read/Write-bit = '0'
4. Auto-Increment-bit - Value of '1' enables auto-increment
5. Memory Address Pointer (MAP) (7-bits) - This is the address of the register to be written to, MSB first.
6. Register Data (8-bits) - MSB First
7. Repeat step 6 if Auto-Increment or bring $\overline{CS}$ HIGH to end operation.

To Read:

1. Bring $\overline{CS}$ low.
2. Chip Address (7-bits) - This should match the RF3002 chip address of 0100000_2.
3. Read/Write-bit = '0'
4. Auto-Increment-bit - Value of '1' enables auto-increment
5. Memory Address Pointer (MAP) (7-bits) - This is the address of the register to be written to, MSB first.
6. Bring $\overline{CS}$ high.
7. Bring $\overline{CS}$ low.
8. Chip Address (same as step 2) - MSB First
9. Read/Write-bit = '1'
10. RF3002 will output 8-bit register value, MSB First, and Increment MAP, if Auto increment enabled.
11. Repeat step 10 for polling or Auto-Increment or bring $\overline{CS}$ high to end operation.

SPI Mode Functional Timing Diagrams

Write

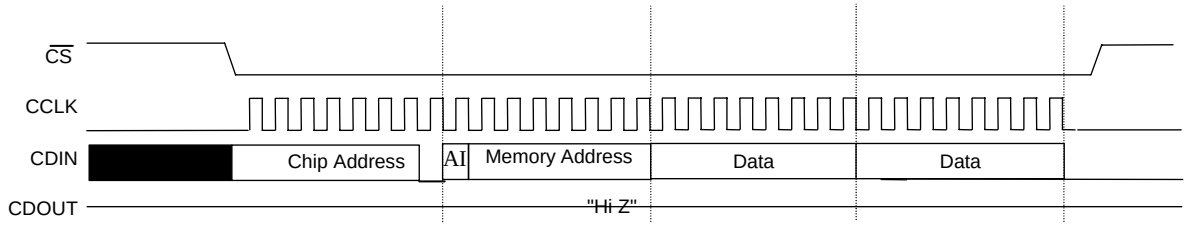


Figure 5. SPI Write Functional Timing Diagram

Read

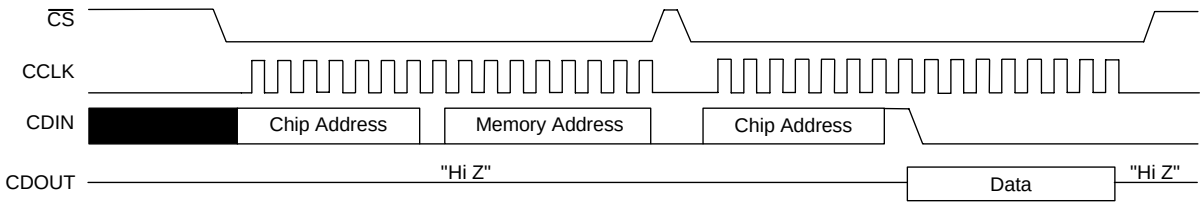


Figure 6. SPI Read Functional Timing Diagram

RF3002 Method of Operation

The transmitter power enable (TX PE) input enables the transmitter process. (Note: Transmit has priority over receive.) When TX PE is high, the LNA GS signal will be driven low. The TX RDY output indicates the readiness of the RF3002 to receive data for transmit. Transmitted data is passed into the RF3002 through the TX DATA input and clocked by the DATA CLK output. The receiver power enable (RX PE) input enables the receiver, and the receive data ready (RX RDY) signal indicates that received data is upcoming. The RF3002 generates the received data clocks, and outputs the received data, through the RX DATA output. The receiver port also provides a clear channel assessment (CCA) to the MAC.

The table below summarizes the operation of the chip. The user should note that RX PE must be High to perform CCA.

TX PE	RX PE	Operation
0	0	Standby mode.
0	1	RX is powered up. CCA circuity is active.
1	0	TX is powered up. Begin TX. CCA is inactive.
1	1	RESERVED

IEEE802.11b Transmit Modes

IEEE802.11b DSSS Transmit Modes

The RF3002 supports PSK and CCK DSSS modes defined in IEEE802.11b specification. The RF3002 also supports the optional short preamble and header format as defined in IEEE802.11b.

The following section describes IEEE802.11b DSSS data transmission. The user must first prepare the applicable control port registers to determine the mode of operation and the transmission length. The mode of operation must be written into Register 1, followed by setting the transmission length (in microseconds). The length is to be written into Registers 17 (bit 0 only), 18 and 19. Mode byte values for IEEE802.11b modes are summarized below

IEEE802.11 DSSS Mode	Mode Byte Value (HEX)
1Mbps DBPSK Long preamble	0x00
1Mbps DBPSK Short preamble	0x10
2Mbps DQPSK Long preamble	0x20
2Mbps DQPSK Short preamble	0x30
5.5Mbps CCK Long preamble	0x40
5.5Mbps CCK Short preamble	0x50
11Mbps CCK Long preamble	0x60
11Mbps CCK Short preamble	0x70

Once the control port values are written, the RF3002 is ready to transmit data. Optionally, the TX length value can be written during the 128μS of preamble. When the user is ready to transmit, TX PE is driven High. This signals the RF3002 to assemble and transmit the 802.11 preamble and header, as described below.

Preamble		Header				Data
128 1's	SFD (16-bits)	Service (8-bits)	Signal (8-bits)	Length (16-bits)	CRC (16-bits)	Data (x-bits)

The preamble and header for 1Mbps mode is always transmitted as 1Mbps BPSK. However for 2Mbps, 5.5Mbps and 11Mbps modes, IEEE802.11b allows a short preamble, which has the preamble, transmitted as 1Mbps BPSK and the header transmitted as 2Mbps QPSK. The usage of the optional short preamble is selected when the transmission mode is written to the control port.

The RF3002 signals that it is nearing the end of the preamble and header transmission by driving TX RDY high. This signals the user that transmission data clocks are coming. When the RF3002 is ready to transmit data it will begin clocking transmit data. Data to be transmitted should be present on TX DATA on the rising edge of DATA CLK. The RF3002 will only clock in the number of data-bits to fill the specified transmission time.

IEEE802.11b DSSS Transmission Summary

1. TX Mode different:
   Write value to the mode register according to table.
2. TX Length different:
   Write the number of uS to transmit in the TX length registers.
3. Drive TX PE High and wait for TX RDY to go High.
4. Transmit data must be valid on the rising edge of DATA CLK.

Figure 7 shows the primary interface mode for the RF3002 TX Data port.

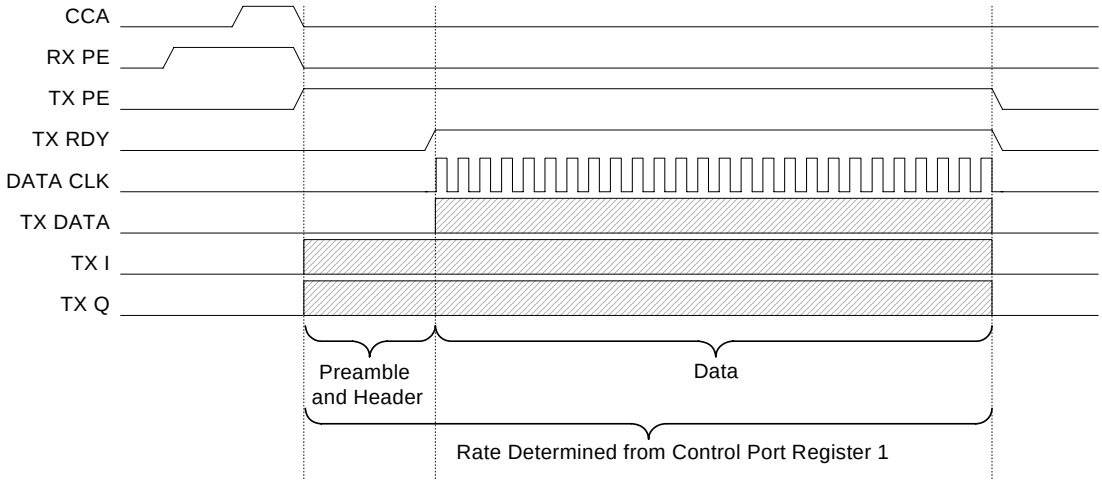


Figure 7. IEEE802.11b Transmit Timing Overview

The RF3002 has provision for an alternate Transmit Data port interface. In the transmit interface an extra clock is asserted after TXRDY goes ‘high' and before the first TX data clock on DATA CLK, see Figure 7a. The alternate Transmit interface is enabled by writing 0x08 into RF3002 Register 0x1C.

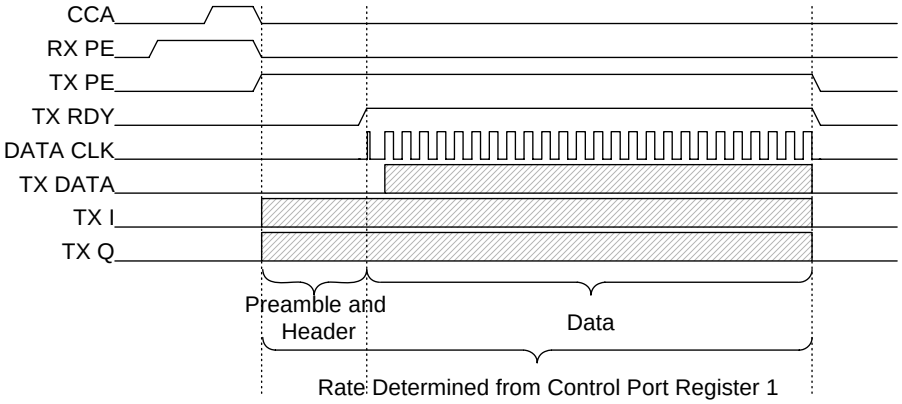


Figure 7a. Alternate Transmit Interface

IEEE802.11b Receive Mode

The RF3002 receiver has an interface similar to the transmit port, and provides link support data through the control port. The user drives RX PE High to enable the receiver circuitry. The RF3002 then begins to watch the incoming data stream for a valid Barker code PN sequence.

The RF3002 contains logic to perform AGC when used in conjunction with the RF2958 as in the RD0316 reference design for IEEE802.11b. The following sections will explain the method of AGC and the calibration hooks that exist inside the RF3002 to compensate for manufacturing tolerances in total system gain of an IEEE802.11b radio.

Diversity

The RF3002 makes diversity decisions every 1mS while looking for A/D saturation according to the state machine in Figure 8.

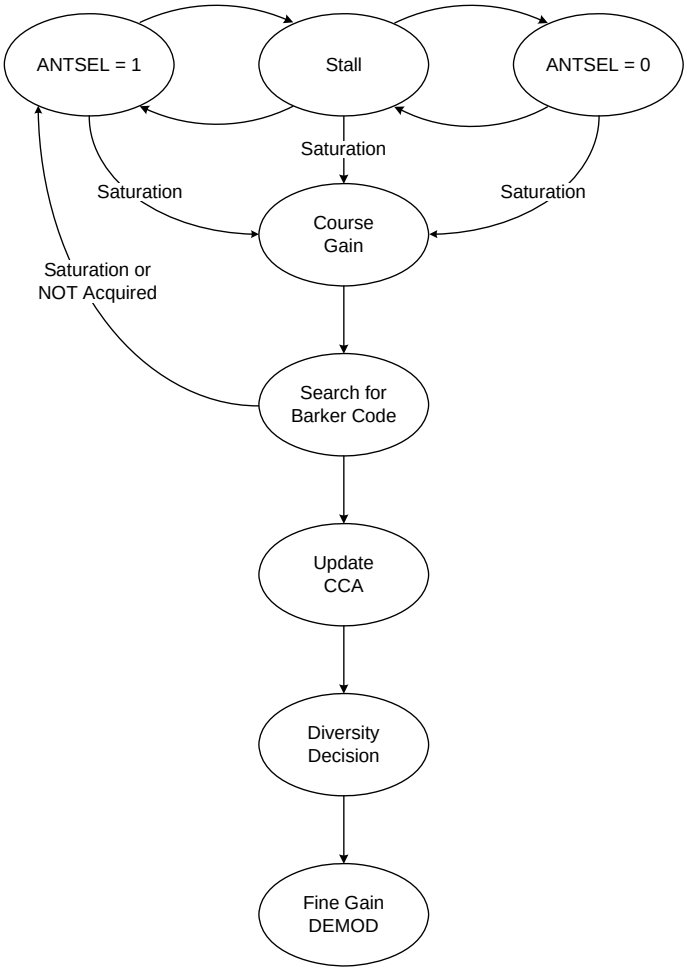


Figure 8. Diversity and AGC Algorithm

AGC Algorithm

The RF3002 AGC algorithm is implemented to automatically control both the RXVGC and the LNAGS pin of the RF2958. The RF3002 is programmed to search the possible gain settings of LNAGS and RXVGC in a binary fashion to quickly determine the final gain setting needed to optimize the inputs to the A/D converters for demodulation. The AGC algorithm is completely controlled by detection of saturation of the A/D converters.

The RF3002 begins the algorithm by setting the RXVGC and LNAGS pins to a predetermined maximum gain condition. Upon detection of A/D saturation, the RF3002 will decrease the system gain (via the RXVGC pin) to a predetermined "mid-point". This mid point is chosen to allow the RF3002 to determine the correct setting of the LNAGS pin. If the RF3002 detects saturation at this "mid-point", the RF3002 will place the RF front end into a low gain mode, and will begin searching for the correct RXVGC setting in a binary tree fashion. If the RF3002 does not detect saturation on the A/D converters while at this "mid-point", the RF3002 will leave the LNAGS pin in high gain mode and proceed with the binary search of RXVGC. This binary tree representation of the gain algorithm can be seen in Figure 9. It is important to note that once the RF3002 makes a decision on the LNAGS setting, that setting will remain for the entire duration of the packet and cannot be altered until the next packet.

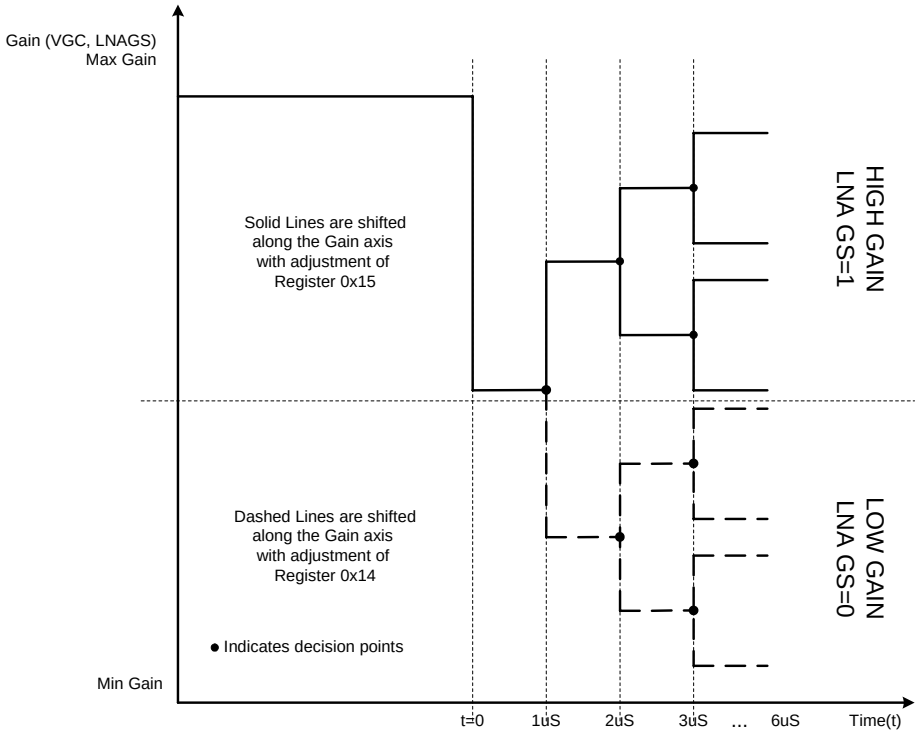


Figure 9. AGC Decision Structure

RSSI is a function of RXVGC and LNAGS. RSSI is updated every 1μS during the AGC algorithm. While demodulating data, the demodulator will make fine tuning adjustments to RSSI based on the value of RXVGC.

The RF3002 is designed to expect 32dB of attenuation in low gain mode. This 32dB can be calibrated to other RF attenuation by adjusting the low gain calibration value in register 20 (0x14).

Post-AGC

When the Barker code is acquired, the RF3002 assigns the ACQ-bit in the mode register to a 1 and proceeds to extract the header information. When the start frame delimiter is identified, the RF3002 will assign a 1 to the SFD-bit in the mode register. The RF3002 will now decode the transmission mode and data length from the header, and check the header via the 16-bit CRC. The RF3002 will then clock-out 32 bits of header information. This will be the 8-bit RX signal field, followed by the 8-bit RX service field, and then the 16-bit RX length field. The MAC can also read these values through the serial port registers 0x04 through 0x07.

The header data will be followed by 16 bit times of no clock transitions.

Immediately before providing data, the RF3002 will drive RX RDY High. The received data will be stable on the rising edge of DATA CLK. In the event the header CRC is incorrect, the RF3002 will bring RX RDY high for the duration of the packet, but no DATA CLK or RX DATA transitions will occur.

IEEE802.11b DSSS Receive Summary

1. Drive RXPE High.
2. RF3002 looks for incoming valid Barker Code.
3. RF3002 sets ACQ bit in Register 0x01.
4. When the Start Frame Delimiter is identified, the RF3002 sets the SFD bit in Register 0x01.
5. RF3002 Extracts Header information.
   This information is copied into the RF3002 RX Status, Service fields and presented on the RXDATA Pin with Clocks on DATA CLK.
6. This will be followed by 16 bit times of no clock transitions.
7. RF3002 Drives RXRDY high, and provides Receive Data on the rising edge of DATA CLK.
8. RF3002 Drives RXRDY low at the end of the data packet.

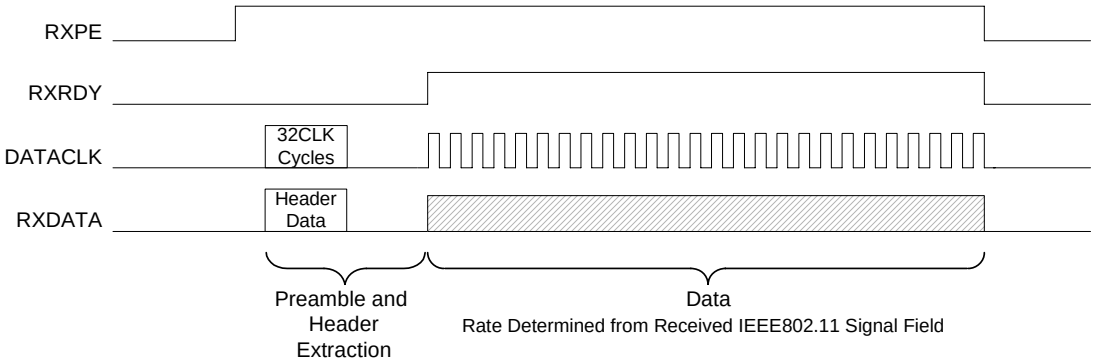


Figure 10. IEEE802.11b Receive Timing Overview

The RF3002 has provision for an alternate Receive Data port interface. In the receiver interface, the DATACLK is inverted, and an extra clock is asserted after RXRDY goes 'low' indicating the end of the received packet, see Figure 13a. The alternate Transmit interface is enabled by writing 0x08 into RF3002 Register 0x1C.

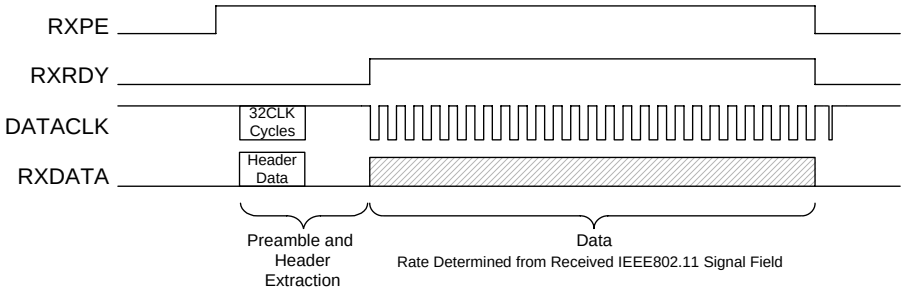


Figure 10a. Alternate Receiver Interface

TX/RX Switch Configuration

The RF3002 supports two different configurations of the TX/RX switch. The default mode is shown in figure 15. Selection of the alternate mode, figure 16, is made by setting the MSB of register 21 (0x15).

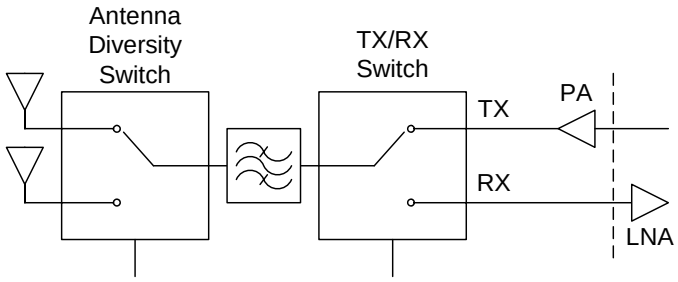


Figure 11. Default Switch Configuration

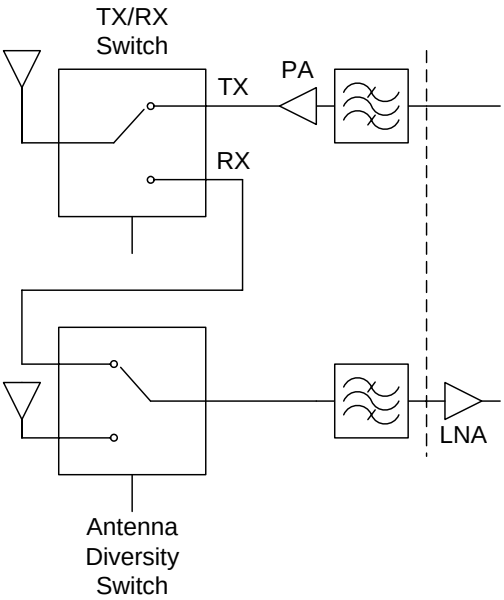


Figure 11a. Alternate Switch Configuration

Block Diagram Breakout

The following sections describe each of the blocks, as indicated in the block diagram, that comprise the RF3002.

Modulator

PSK Modes

The RF3002 uses a proprietary architecture that allows the modulation of PSK signals by simply reprogramming the part via the control port. The transmitted data stream is first spread and the resulting data stream is modulated.

CCK Mode

IEEE802.11b Preamble/Header Creation and Assembly

The RF3002 provides circuitry to generate and assemble a preamble and header as specified in the IEEE802.11b specification. The short preamble option for 2Mbps, 5.5Mbps and 11Mbps, as specified in IEEE802.11b, is selectable in the mode control register. The RF3002 will transmit these fields along with a protective CRC-16 for error detection. For other protocols, the preamble/header circuitry is disabled, and packet structures should be generated externally.

Demodulator

PSK Modes

The RF3002 uses a proprietary architecture that allows the demodulation of PSK signals by simply reprogramming the part via the control port. The received signal is first de-spread and the PSK signal is recovered.

CCK Mode

In order to perform CCK demodulation, circuitry is provided to pass the output of the A/D converters to a fast Walsh transform (FWT). The output of the FWT is then passed to decision circuitry to determine the received signal.

IEEE802.11b Preamble/Header Detection and Extraction

Circuitry is provided to search the incoming data for start frame delimiter (SFD) and to obtain length field information as well as modulation type. In 802.11 modes, this circuitry is always active since the preamble and header tells the PHY which modulation type the data packet is using. The RF3002 will also check the preamble/header field for errors by checking the CRC-16 field for errors.

Data Converters

The RF3002 contains all A/D converters and D/A converters required to implement a transceiver.

A/D Converters

I/Q A/Ds - These are 5-bit analog-to-digital converters used to sample the data according to the mode of the RF3002.

D/A Converters

Four (4) digital-to-analog converters are present for transmitter VGC, receiver VGC, I Out, and Q Out.

RSSI, CCA and AGC

Scramblers

Scramblers for whitening the spectrum are provided, as specified in IEEE802.11b.

SCRAMBLER NOTE: The data scrambler defined by IEEE802.11b has a probability of 1/128, to lock up scrambling when random data is followed by a repetitive pattern. The patterns identified are: all 0's; all 1's; repetitive 01's; repeated 0011's; and, repeated 000111's. Once the pattern ceases the scrambler will resume its normal operation.

Diversity
Switching and detection at beginning of Receive.

Equalizer
For multipath cancellation, the RF3002 defines the path with the largest magnitude as the main path and all others as secondary paths. The RF3002 equalizer can cancel the three most significant secondary paths. These can either be three (3) post-cursor, echo paths, or they can be two (2) post-cursor and one (1) pre-cursor paths. Pre-cursor delay can be up to one-quarter symbol period. Post-cursor delay can be up to one-half (1/2) symbol period. The magnitude of cancelled multipaths up to -0.5dBc, normalized to the main path.

Control Port Register Definitions for RF3002

Register 0x00 - Reserved

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'

This register is reserved.

Register 0x01 - Modem Control and RX Status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode 3	Mode 2	Mode 1	Mode 0	Short Preamble*	ACQ *	SFD *	CRC *

* - Read Only

This register is used to setup primary operation of the modem.

NOTE: The four (4) LSB's are read-only and reflect the receiver status.

Mode (3-0) - TX Mode

Mode 3	Mode 2	Mode 1	Mode 0	Mode ID	Notes
0	0	0	0	802.11 1Mbps DSSS	Long preamble. Default Mode
0	0	0	1	1Mbps DSSS	Short preamble
0	0	1	0	802.11 2Mbps DSSS	Long preamble
0	0	1	1	802.11 2Mbps DSSS	Short preamble
0	1	0	0	802.11 5.5Mbps CCK	Long preamble
0	1	0	1	802.11 5.5Mbps CCK	Short preamble
0	1	1	0	802.11 11Mbps CCK	Long preamble
0	1	1	1	802.11 11Mbps CCK	Short preamble
1	0	0	0	BPSK	Reserved
1	0	0	1	QPSK	Reserved
1	0	1	0	Reserved	Reserved
1	0	1	1	Reserved	Reserved

Default 802.11 1Mbps DSSS, RX mode detected automatically.

NOTE: In 802.11 modes, the received data rate will be accepted from the received header and therefore will be selected automatically.

Short Preamble - READ ONLY
- 0 - Long Preamble Received
- 1 - Short Preamble Received

ACQ - Receiver acquisition status - READ ONLY
- 0 - Not locked
- 1 - acquired

SFD - 802.11 SFD status - Read Only
- 0 - Not found
- 1 - SFD detected

CRC - 802.11 RX CRC - Read Only
- 0 - CRC valid
- 1 - CRC error

Register 0x02 - CCA Control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CCA1	CCA0	RSSI_t5	RSSI_t4	RSSI_t3	RSSI_t2	RSSI_t1	RSSI_t0

CCA1, CCA0 - 802.11 CCA Mode

CCA1	CCA0	CCA Mode
0	0	RSSI Threshold Sensitive
0	1	Acquisition Sensitive
1	X	Both

RSSI_t - 6-bit RSSI threshold value for CCA.

Register 0x03 - Diversity and RSSI Value

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Diversity	Cpantsel	RSSI5 *	RSSI4 *	RSSI3 *	RSSI2 *	RSSI1 *	RSSI0 *

***** - Read Only
NOTE: The six (6) LSB's are read-only and reflect the receiver status.

Diversity - RX diversity enable bit.
Default -
0 - No diversity, ANT SEL pin is forced to Cpantsel.
1 - Diversity active, RF3002 automatically selects ANT SEL pin.
Cpantsel - Antenna selection bit in non-diversity mode.
Default -
0 - ANT SEL forced to 0.
1 - ANT SEL forced to 1.
RSSI5-0 - Output of the RSSI A/D - Read Only

Register 0x04 - RX Signal Field (Read only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_Sig7	RX_Sig6	RX_Sig5	RX_Sig4	RX_Sig3	RX_Sig2	RX_Sig1	RX_Sig0

In DSSS modes, this value is the received byte of the received signal field. In FHSS, only the four (4) LSB's are used.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Received Mode
0	0	0	0	1	0	1	0	1Mbps DSSS
0	0	0	1	0	1	0	0	2Mbps DSSS
0	0	1	1	0	1	1	1	5.5Mbps DSSS
0	1	1	0	1	1	1	0	11Mbps DSSS
0	0	0	0	0	0	0	0	Reserved
0	0	0	0	0	0	0	1	1.5Mbps FSK***
0	0	0	0	0	0	1	0	Reserved
0	0	0	0	0	0	1	1	2.5Mbps FSK***
0	0	0	0	0	1	0	0	3Mbps FSK***
0	0	0	0	0	1	0	1	3.5Mbps FSK***
0	0	0	0	0	1	1	0	4Mbps FSK***
0	0	0	0	0	1	1	1	4.5Mbps FSK***

*** - IEEE802.11b proposed modulation rates not currently supported.

Register 0x05 - RX Length Field MSB's (Read only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_LN15	RX_LN14	RX_LN13	RX_LN12	RX_LN11	RX_LN10	RX_LN9	RX_LN8

The upper byte of the length field received.
In DSSS mode, this value is the length in microseconds of the received data packet.

Register 0x06 - RX Length Field LSB's (Read only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_LN7	RX_LN6	RX_LN5	RX_LN4	RX_LN3	RX_LN2	RX_LN1	RX_LN0

The lower byte of the length field received.

Register 0x07 - RX Service Field (Read only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RX_SER7	RX_SER6	RX_SER5	RX_SER4	RX_SER3	RX_SER2	RX_SER1	RX_SER0

This register is used per IEEE802.11b specification.
RX_SER7 is length field extension in high data rate proposal 802.11b.
RX_SER3 is modulation selection bit for high rate transmission.
0 - CCK
RX_SER2 signifies Synth Clock to Signal Clock per 802.11 specification.

Register 0x08 - Reserved

Register 0x09 - Reserved

Register 0x0A - Reserved

Register 0x0B - Reserved

Register 0x0C - Reserved

Register 0x0D - Reserved

Register 0x0E - Reserved

Register 0x0F - Reserved

Register 0x10 - Reserved

Register 0x11 - TX Variable Gain and TX Length Field Extension

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TXVGC5	TXVGC4	TXVGC3	TXVGC2	TXVGC1	TXVGC0	SCRAMBLER	TX_LN16

TXVGC5-TXVGC0 - Gain setting for transmission.

000000 - Min gain

111111 - Max gain

SCRAMBLER - This bit enables and disables the IEEE802.11b data scrambler.

Bit Value	Scrambler Mode
0	Enabled
1	Disabled

TX_LN16 - TX length extension bit as defined in IEEE 802.11b specification.

Register 0x12 - TX Length Field MSB's

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_LN15	TX_LN14	TX_LN13	TX_LN12	TX_LN11	TX_LN10	TX_LN9	TX_LN8

Register 0x13 - TX Length Field LSB's

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TX_LN7	TX_LN6	TX_LN5	TX_LN4	TX_LN3	TX_LN2	TX_LN1	TX_LN0

Registers 0x12 and 0x13 indicate the number of microseconds that the RF3002 is to transmit after receiving a request to start transmission.

Register 0x14 - Options Register 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Switch Option	TX_Filter_ Enable	Low_Gain5	Low_Gain4	Low_Gain3	Low_Gain2	Low_Gain1	Low_Gain0

Bit 7: Switch Option - a value of '1' selects alternate switch configuration

Bit 6: TX Filter Enable

Bit 5 .. Bit 0: Low Gain Calibration

Register 0x15 - Options Register 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CH 14	DSSS PAD	Hi_Gain5	Hi_Gain4	Hi_Gain3	Hi_Gain2	Hi_Gain1	Hi_Gain0

Bit 7: Option for Japanese channel 14.

Bit 6: 6dB pad of DS modes

Bit 5 .. Bit 0: High gain calibration for optional manual AGC

Register 0x16 - Options Register 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED'0'	FINE_TUNE[1]	FINE_TUNE[0]	DC Offset Mode	DC Offset Mode	ACQ_THRESH	ACQ_THRESH	ACQ_THRESH

Bit 7: Reserved, set to '0'

Bit 4	Bit 3	DC Offset Mode
0	0	Primary
0	1	Both
1	0	None
1	1	Secondary

Bit 6	Bit 5	Description
0	0	Default saturation-based RXVGC fine tune mode.
0	1	Alternative gain fine tune.
1	0	Alternative gain fine tune +2.7dB.
1	1	Alternative gain fine tune +4.0dB.

Bit 2	Bit 1	Bit 0	Acquisition Threshold
0	0	0	Default Value
0	0	1	1.25xDefault Value
0	1	0	1.5xDefault Value
0	1	1	1.75xDefault Value
1	0	0	2.0xDefault Value
1	0	1	0.25xDefault Value
1	1	0	0.5xDefault Value
1	1	1	0.75xDefault Value

Register 0x17 - Reserved

Register 0x18 - Reserved

Register 0x19 - Reserved

Register 0x1A - Reserved

Register 0x1B - Reserved

Register 0x1C - Options Register 4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAT_THRESH [2]	SAT_THRESH [1]	SAT_THRESH [0]	Enable High Gain Calibration	Enabled Alternative Data Port Interface	RESERVED'0'	RESERVED'0'	RESERVED'0'

Bit 7 .. Bit 5: Signed Magnitude Offset for all steps of coarse AGC. Saturation threshold is V+4 value where V=-3≤V≤+3, in 2's complement.

Bit 4: A value of '1' disables automatic high gain calibration. Enabling manual calibration with Reg 0x15[5:0].

Bit 3: A value of '1' enables the alternate TX/RX data bus interface.

Bit 2 .. Bit 0: Reserved, set to '0'.

Register 0x1D - Options Register 5

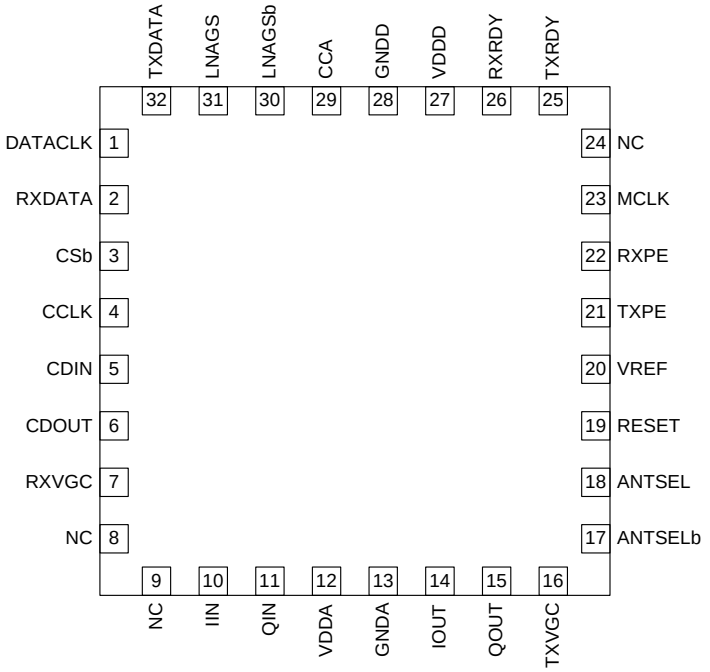
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'	RESERVED'0'	AGC Re-trigger Threshold	RESERVED'0'	RESERVED'0'

Bit 7 .. Bit 3: Reserved, set to '0'.
Bit 2: Sets threshold for AGC re-trigger.
'0' sets re-trigger threshold to high count.
'1' sets re-trigger threshold to low count.
Bit 1: Reserved, set to '0'.
Bit 0: Reserved, set to '0'.

Register 0x1E - Reserved

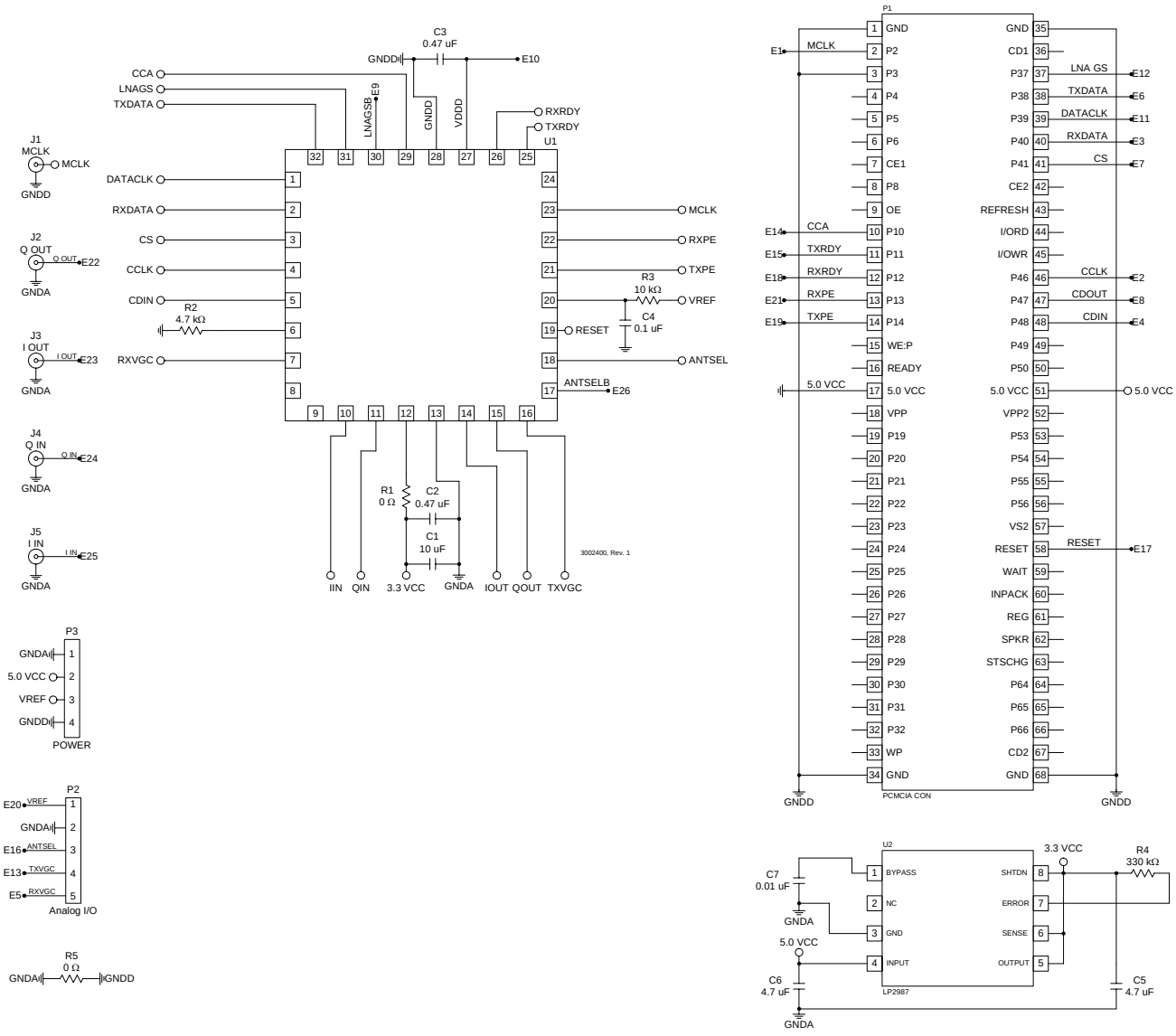
Register 0x1F - Reserved

Pin Out


TXDATA 32
LNAGS 31
LNAGSb 30
CCA 29
GNDD 28
VDDD 27
RXRDY 26
TXRDY 25
DATACLK 1
RXDATA 2
CSb 3
CCLK 4
CDIN 5
CDOUT 6
RXVGC 7
NC 8
24 NC
23 MCLK
22 RXPE
21 TXPE
20 VREF
19 RESET
18 ANTSEL
17 ANTSELb
9 NC
10 IIN
11 QIN
12 VDDA
13 GNDA
14 IOUT
15 QOUT
16 TXVGC

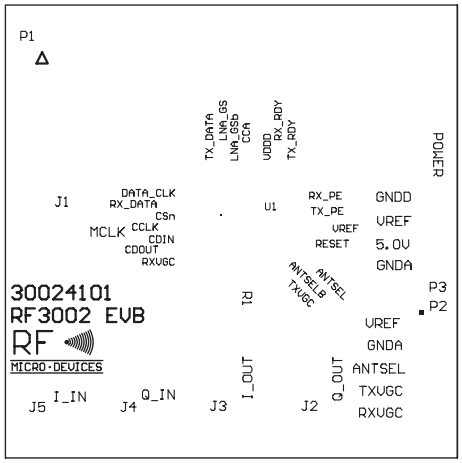
Evaluation Board Schematic

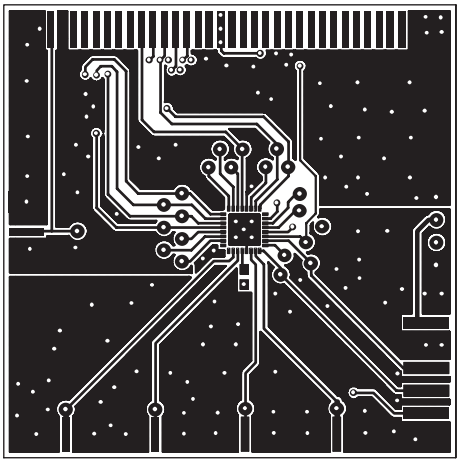
(Download Bill of Materials from www.rfmd.com.)

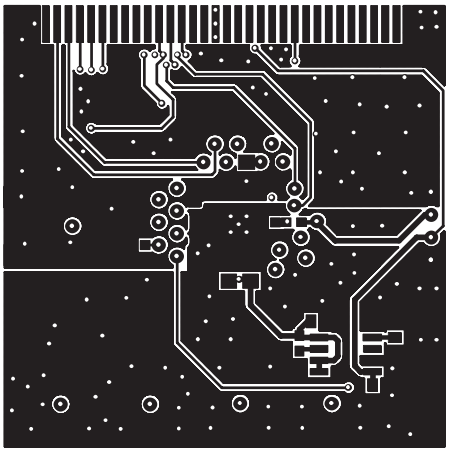


Evaluation Board Layout
Board Size 2.12” x 3.57”

Board Thickness 0.062”, Board Material FR-4

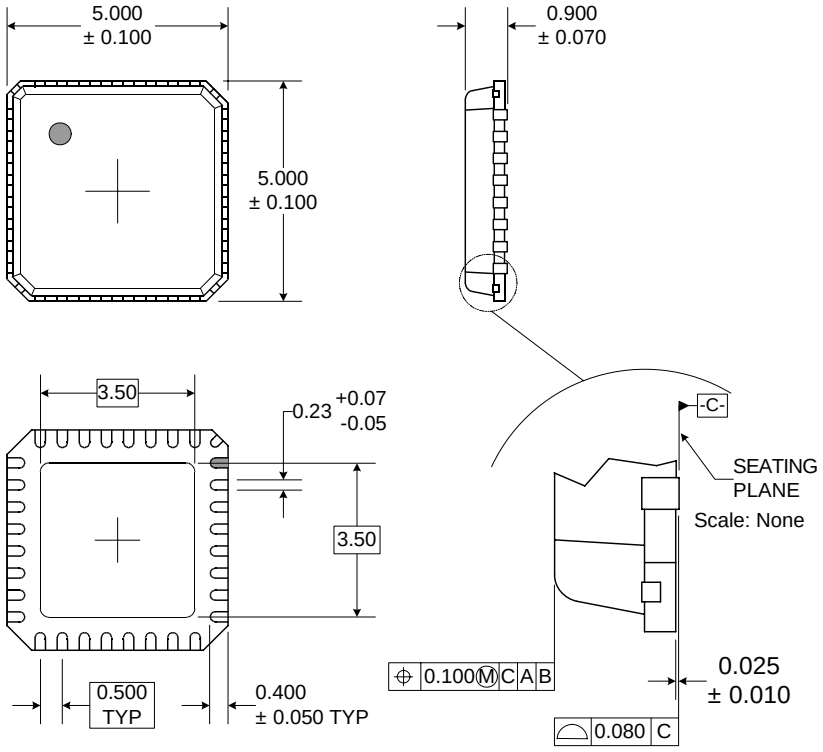






Package Drawing

QFN, 32-pin, 5x5



PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

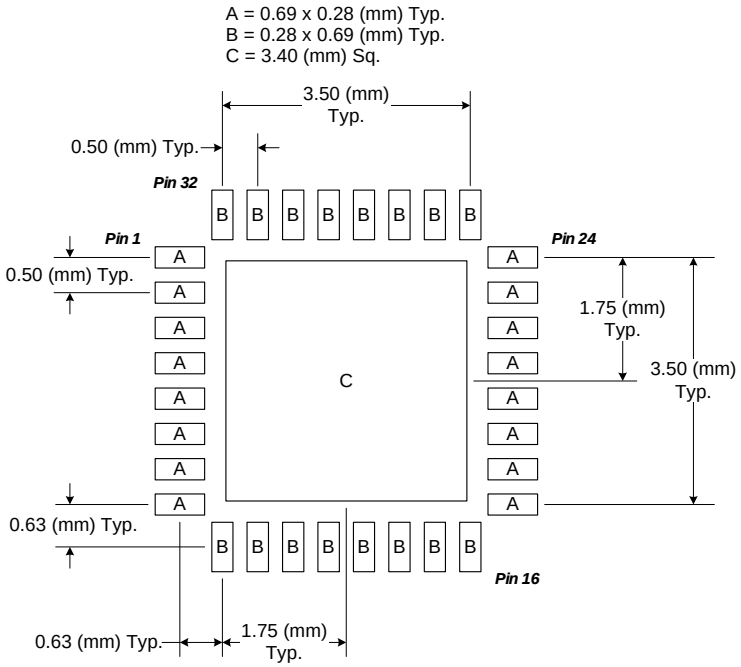


Figure 17. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

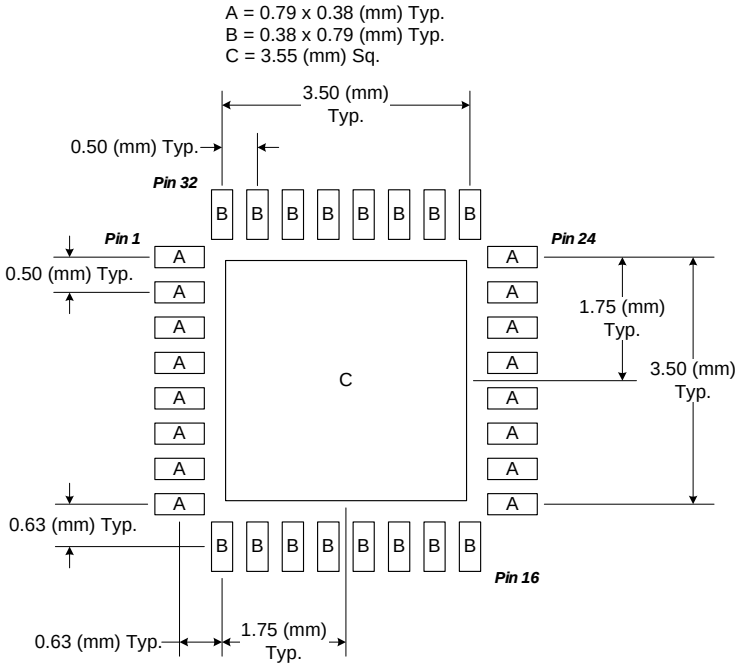


Figure 18. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB Metal Land Pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.