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RF9008

2.4GHz SPREAD-SPECTRUM TRANSCEIVER

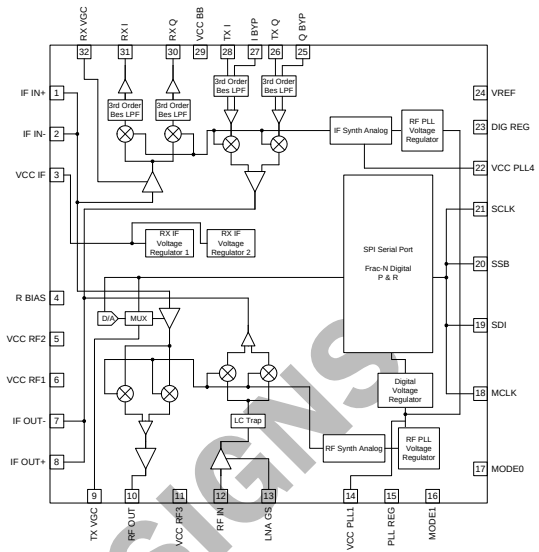
RoHS Compliant & Pb-Free Product
Package: QFN, 32-Pin, 5x5 (Supplier 1)

Features

- Complete IEEE802.11 Transceiver including VCO's
- Small 32-pin Leadless Package
- Minimal External Components Required
- Low Receive Current
- High Performance Super-het Architecture

Applications

- IEEE 802.11 WLANs
- High Speed Digital Links
- Wireless Security
- Low-Power QPSK Links



Functional Block Diagram

Product Description

The RF9008 is a single-chip transceiver specifically designed for IEEE 802.11 applications. The RF9008 part includes all required transceiver functions. The receiver includes: an LNA and downconverter; complete synthesizers and VCO's; direct conversion from IF receiver with variable gain control; quadrature demodulator; I/Q baseband amplifiers; and, on-chip baseband filters. For the transmit side, a QPSK modulator and upconverter are provided along with the synthesizer, VCO, and PA driver. A minimum number of external components are required, resulting in an ultra-compact low-cost radio design. Two-cell or regulated three-cell (3.6V maximum) battery applications are supported by the part. The RF9008 is also part of a 2.4GHz chipset along with our high-efficiency GaAs HBT PA and the RF3002 Baseband Processor.

Ordering Information

RF9008TR13	2.4GHz Spread-Spectrum Transceiver (Tape & Reel)

Optimum Technology Matching® Applied

☐ GaAs HBT	☑ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Control Voltages	-0.5 to +3.6	V_{DC}
Input RF Level	+12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Receiver LNA/RF					V_{CC}=2.8V, T=+25°C, MCLK=44MHz, RXVGC=1.6V, unless otherwise specified
RF Frequency Range	2400		2500	MHz	Note 1
IF Frequency Range	363		385	MHz	Note 1, 374MHz ±11MHz
Voltage Gain - High	29 (17dB power)	32 (20dB power)	35 (23dB power)	dB	LNA/mixer voltage gain (Note: into output impedance). LNA/mixer/SAW filter voltage gain. LNA GS=1
Voltage Gain - Low	-5 (-16dB power)	-2 (-13dB power)	+1 (-10dB power)	dB	LNA/mixer voltage gain. LNA GS=0
Noise Figure - High Gain	3.5	4.0	4.5	dBm	Note 1
Noise Figure - Low Gain	28	32	36	dBm	Note 1
Input IP3 - High Gain	-20.0	-18.0	-17.5	dBm	Note 1
Input IP3 - Low Gain	+8.0	+15.0	+18.0	dBm	Note 1
Input P1dB - High Gain	-30.0	-28.0	-26.0	dBm	Note 1
Input P1dB - Low Gain	-2.0	+7.0	+10.0	dBm	Note 1
Input Return Loss		10		dB	Z_0=50Ω
Output Impedance		750		Ω	
Image Rejection	30	39		dB	Note 2
Receiver IF VGA/Baseband					
IF Frequency Range		374		MHz	Note 1
IF Input Impedance		820		Ω	
Voltage Gain - High	65		71	dB	V_{GC}=1.25V (measured to single-ended output)
Voltage Gain - Low	2		4	dB	V_{GC}=1.95V (measured to single-ended output)
Gain Accuracy	-3		+3	dB	Note 1. For a given RX VGC voltage, the measured gain should lie within ±3dB of ideal.
Gain Response Time			300	ns	Measured with a DC step from 1.3V to 1.8V to 90% final value (within 1dB)
Gain Flatness	-0.25		+0.25	dB	Note 1. 374MHz ±11MHz, relative to gain at 374MHz
Input V1dB	480	500	520	mV_{P-P}	Note 1. 1dB compression of IF strip.
Output Distortion		1.0	2.0	%	Note 1. RX I or Q, single-ended.
Output Voltage		0.75		V_{P-P}	Note 1. RX I or Q, single-ended.
Output V1dB	1.25			V_{P-P}	Note 1. RX I or Q, single-ended.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Receiver IF VGA/Baseband, cont'd					
Group Delay		15		ns	
Output Impedance		20		Ω	
I/Q Magnitude Error	-0.35		+0.35	dB	Note 1, 2. Measured at 500kHz offset.
I/Q Phase Error	-3.0		+3.0	°	Note 1, 2. Measured at 500kHz offset.
I/Q DC Offset		7	20	mV	Note 2. Systematic offset. S_{QRT} $[(V_{OUTI}-V_{REF})^2+(V_{OUTQ}-V_{REF})^2)]$
Transient DC Step			40	mV	VGC step 1.3V to 1.8V, P_{IN}=-50dBm
V_{REF}	1.65	1.7	1.75	V	Note 2.
V_{REF} Maximum Output Current	1.0			mA	Note 1, Source current
Transmitter Modulator/Baseband					
I/Q Magnitude Error	-0.35		+0.35	dB	Note 1, 2. Measured at 500kHz offset.
I/Q Phase Error	-3.0		+3.0	°	Note 1, 2. Measured at 500kHz offset.
Input Signal (Single-Ended)		300	330	mV_{P-P}	Note 1. Input level to maintain linearity
Voltage Gain to IF	3	5	7	dB	Note 1. Measure from complex magnitude to IF V_{P-P}
Output SNR		32		dB	Note 1. Connected to SAW filter.
Carrier Leakage		-26	-17	dBc	Note 1.
VGA Driver/Upconverter					
Input P1dB	550			mV_{P-P}	Note 1. 6dB from max input
Minimum Gain			0	dB	Note 1. TX VGC at 1.3V
Maximum Gain	17			dB	Note 1. TX VGC at 1.9V
Image Rejection	30	50		dBc	
RF LO Leakage	-25	-36		dBm	F_{LO}=2048MHz to 2110MHz
Minimum Output Power			-12	dBm	Note 2. TXVGC=1.3V
Maximum Output Power	0	1.5		dBm	Note 2. TXVGC≤1.9V, TX I/Q=300 mV_{P-P}, 802.11 spectral mask compliant
	1.4	2.4		dBm	Note 2. TXVGC=1.9V, TX I/Q=300 mV_{P-P}, Not guaranteed to mask compliance
Output Power Variance		±2	±2.5	dB	Note 1. 802.11 Spectral Mask, V_{CC}=2.8V±0.1V. TX I/Q=300 mV_{P-P}±10%. Temperature compensated per schematics as shown.
PLL Lock Time					CAL1 register=0X3FFFA (max values)
Turn-on Lock Time		0.7	1.5	mS	Note 1. From RESET mode to IDLE/RX/TX mode to calibration complete and PLL locked.
Channel Changing Lock Time		0.7	1.0	mS	Note 1. Change from any channel to any channel. Measured from SSB going high to calibration complete and PLL locked.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Digital Input Specifications					
Apply to pins: SSB, SDI, SCLK, MODE0, MODE1, MCLK					
Input High Voltage (V_{IH})	$0.7V_{DD}$			V	
Input Low Voltage (V_{IL})			$0.3V_{DD}$	V	
Input High Static Current (I_{IH})			5	µA	
Input Low Static Current (I_{IL})			5	µA	
Reset Time		50		µs	Exiting Reset mode or using SPI Reset
Apply to pins: SSB, SDI, SCLK					
Input Setup Time (T_{SU})	5			ns	Note 3.
Input Hold Time (T_{HLD})	5			ns	Note 3.
Input Rise/Fall Time (T_{RFI})			5	ns	
Input Clock to Select Time (T_{CS})	5			ns	
Input Clock Pulse Width High (T_{CWH})	22			ns	
Input Clock Pulse Width Low (T_{CWL})	22			ns	
PLL Recalibration Pulse Width (T_{RC})	1/fr			s	For f_r=44MHz, T_{RC} is 22.7ns
Digital Driver Output					
Apply to pin: SDI (output mode)					
Output High Voltage (V_{OH})	$0.8V_{DD}$			V	Note 1. With 1mA load
Output Low Voltage (V_{OL})			$0.2V_{DD}$	V	Note 1. With 1mA load
Output Rise/Fall Time (T_{RFO})			5	ns	Note 1. With 20pF maximum load capacitance measured from 10% to 90% of output voltage.
Output to Hi Z (T_{HIZ})		10		ns	Note 1. Time from SSB going high to when SDI is high impedance.
Output Current Source ($\|I_{OH}\|$)	3.8			mA	Output at (V_{DD}-0.3V)
Output Current Sink ($\|I_{OL}\|$)	10			mA	Output at 0.3V
MCLK Input					
Duty Cycle	40		60	%	Note 1. Freq=22MHz or 44MHz.
Input High Voltage (V_{IH})	1.2		V_{DD}	V	Note 1.
Input Low Voltage (V_{IL})	0		0.3	V	Note 1.
Input Voltage (V_{P-P})	500		1200	mV_{P-P}	Note 1. AC-coupled, internal DC bias.
DC Bias at MCLK (MCLK_DC)	0.6		1.1	V	
Specification Valid Range					
Temperature	-10		+60	°C	
Supply Voltage	2.7	3.3	3.6	V	
Transmit Current	44	61	70	mA	Note 2. MODE0=0, MODE1=1
Receive Current	27	43	53	mA	Note 2. MODE0=1, MODE1=0
Idle Current	5	25	35	mA	Note 2. MODE0=0, MODE1=0
Reset Current		1	2	mA	Note 2. MODE0=1, MODE1=1
Hibernate Current		0.2	0.5	mA	Note 2.
NOTES					
1. Specifications guaranteed by design and characterization, but not tested for 0°C to 60°C and V_{CC}=2.7V-3.6V.					
2. Production tested at V_{CC}=2.8V, +25°C.					
3. Setup and Hold Times are measured from the time where the waveforms cross $V_{DD}/2$.					

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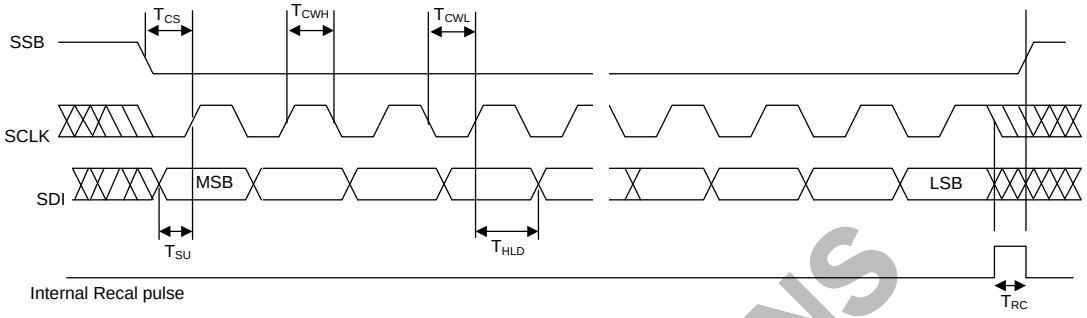
Digital Timing Specifications



Pin	Function	Description
1	IF IN+	Differential input from IF SAW filter. See application schematic for matching circuit.
2	IF IN-	See pin 1.
3	VCC IF	Power supply for IF circuitry. Provide 330pF bypass capacitor close to this pin.
4	R BIAS	Bandgap voltage reference for on-chip biasing. Install a 22.1kΩ, 1% resistor from this pin to ground.
5	VCC RF2	Power supply for TX and RX bias, LO buffers and mixers. Provide 6pF bypass capacitor close to this pin.
6	VCC RF1	See pin 5.
7	IF OUT-	Differential output to IF SAW filter. See application schematic for matching circuit.
8	IF OUT+	See pin 7.
9	TX VGC	TX analog gain control. Depending on desired operation mode, transmitter gain can be controlled through this pin or the three-wire digital interface. This pin can also provide a bias voltage to an external PA. See theory of operation for details.
10	RF OUT	TX PA driver output.
11	VCC RF3	Power supply for LNA and TX output driver. Power should be connected to this pin through an inductor or a long 50Ω transmission line RF-shorted with a 6pF capacitor at the other end.
12	RF IN	RX input from antenna.
13	LNA GS	Gain select pin for the internal LNA. High-gain operation is selected when this pin is a logic '1'.
14	VCC PLL1	Power supply for the PLL RF LO synthesizer. Provide 0.01μF and 6pF bypass capacitors close to this pin.
15	PLL REG	Internal PLL regulator output. Bypass with 10nF capacitor. Do not connect to V_{CC} or ground.
16	MODE1	Controls operational state of the device. See Theory of Operation section for details.
17	MODE0	See pin 16.
18	MCLK	Reference oscillator for the PLL synthesizer.
19	SDI	Data signal for the synchronous three-wire digital control interface.
20	SSB	Chip select signal for the synchronous three-wire digital control interface.
21	SCLK	Clock signal for the synchronous three-wire digital control interface.
22	VCC PLL4	Power supply for the PLL IF LO synthesizer. Provide 0.01μF and 330pF bypass capacitors close to this pin.
23	DIG REG	Internal digital regulator output. Bypass with 10nF capacitor. Do not connect to V_{CC} or ground.
24	VREF	I/Q DC reference voltage for the baseband processor. This pin should be connected to a high impedance on the baseband processor.
25	Q BYP	Baseband differential input signal for the TX quadrature channel. For single-ended applications, bypass to ground with a 0.01μF capacitor.
26	TX Q	Baseband input signal for the TX quadrature channel.
27	I BYP	Baseband differential input signal for the TX in-phase channel. For single-ended applications, bypass to ground with a 0.01μF capacitor.
28	TX I	Baseband input signal for the TX in-phase channel.
29	VCC BB	Power supply for baseband circuitry. Provide 0.01μF bypass capacitor close to this pin.
30	RX Q	Baseband output signal for the RX quadrature channel.
31	RX I	Baseband output signal for the RX in-phase channel.
32	RX VGC	Analog gain control for the RF IF amplifier.
Pkg Base	GND	Device ground. Connect directly to PCB ground plane.
	ESD	All pins except pin 12 are provided with electrostatic discharge protection to 3kV using the human body model.

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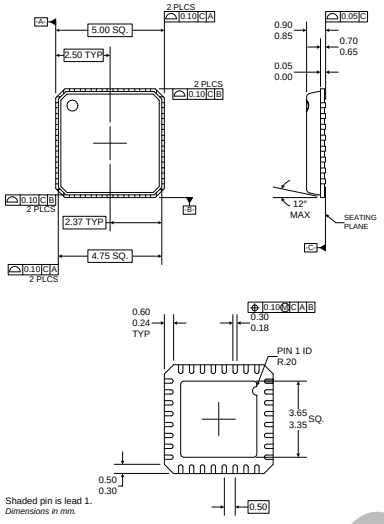
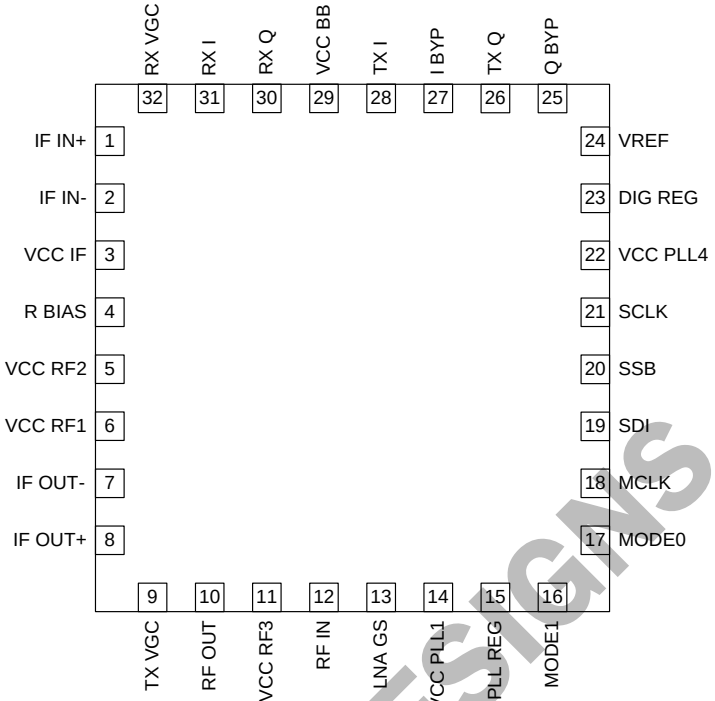
Package Drawing



Pin Out



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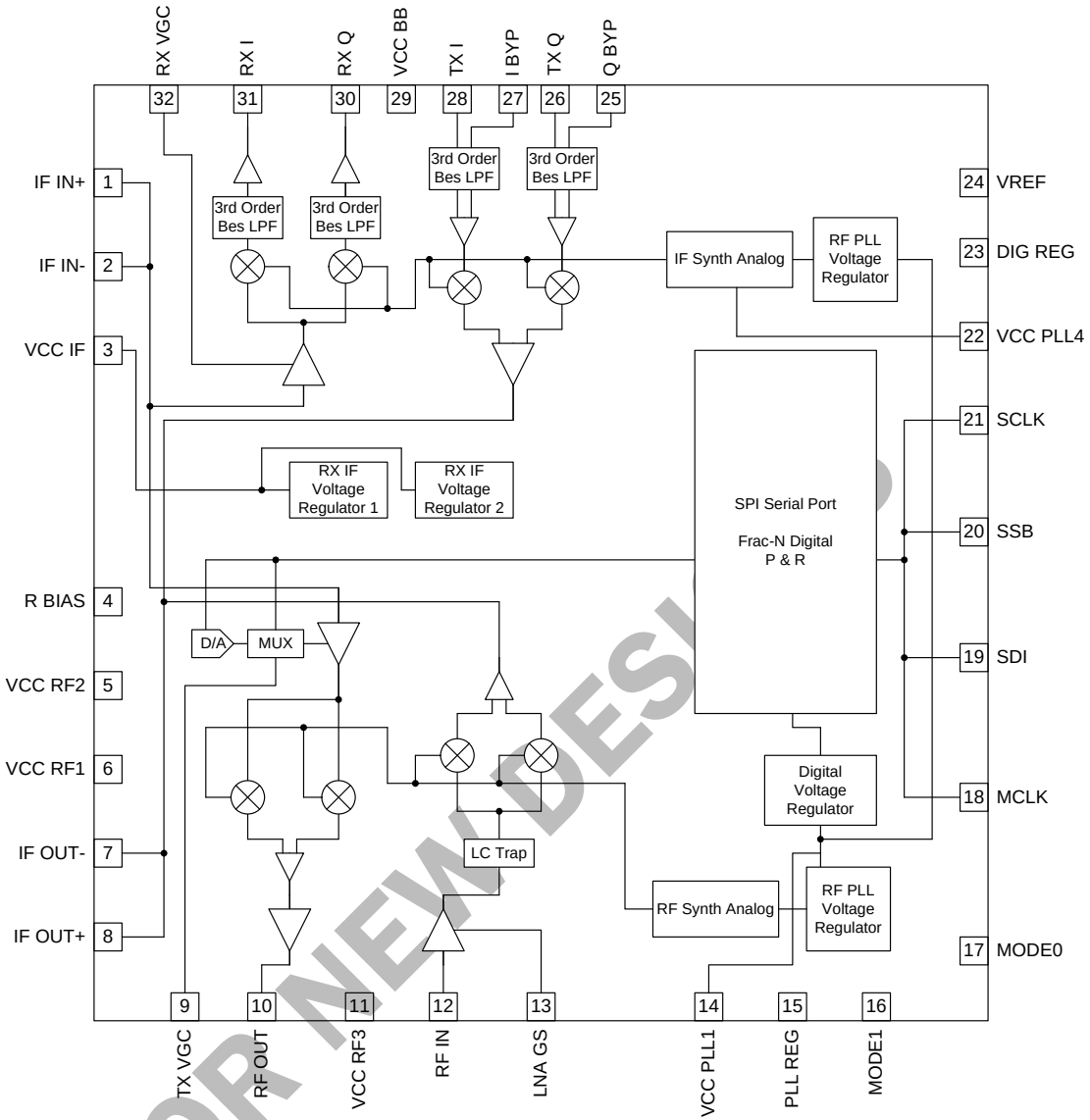
Detailed Functional Block Diagram



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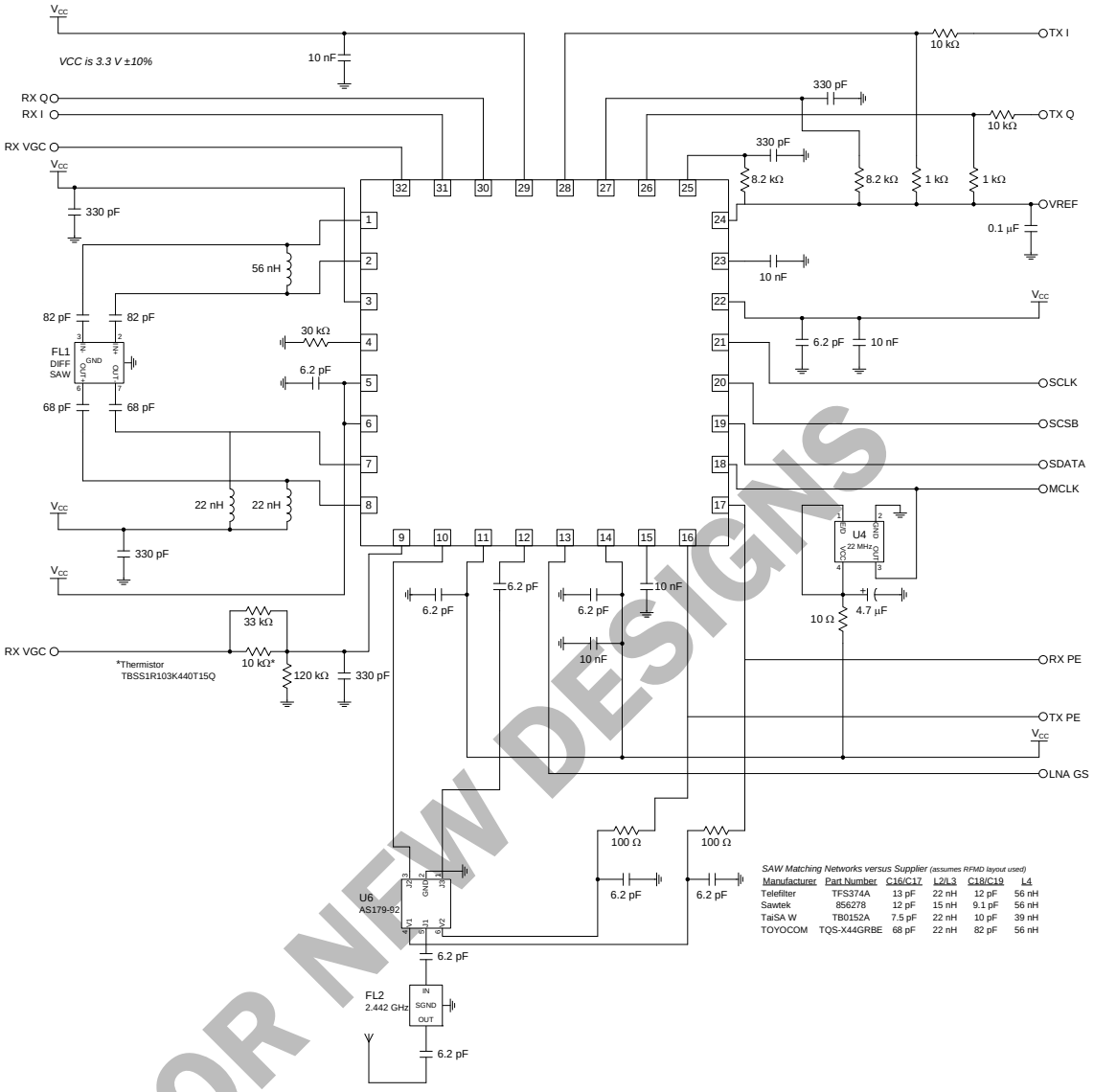
Application Schematic



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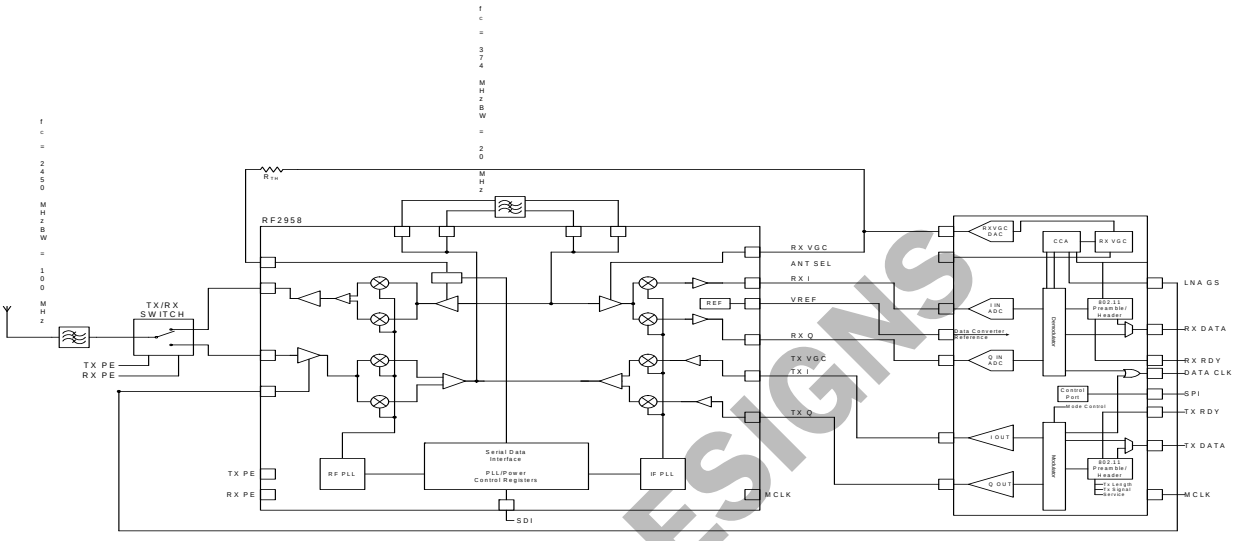
Theory of Operation

The RF9008 is a single-chip transceiver designed specifically for IEEE 802.11 wireless LAN applications. In addition to typical transceiver functions of RF conversion of both the transmit and receive signals, the RF9008 incorporates a low-noise amplifier (LNA) and a dual phase-locked loop (PLL) frequency synthesizer to reduce end-product component count and to simplify integration into end-products. The RF9008 uses a superheterodyne frequency conversion architecture in both the transmit and receive signal paths for superior performance in 802.11 applications. It also incorporates power conservation functionality to increase battery life in portable and mobile applications.



SYSTEM ARCHITECTURE

The overall system architecture is based around a superheterodyne conversion process. For the transmitter side, the baseband in-phase (I) and quadrature (Q) signal components are converted to an intermediate frequency (IF) of 374MHz. An external SAW filter is used to filter out undesired spurious frequencies. The IF is then converted to the over-the-air radio frequency (RF) between 2.412GHz and 2.483GHz using low-side injection. The TX RF output is followed by a TX/RX switch and a band pass filter which eliminates the undesired sideband resulting from the mixing process before broadcasting the signal through the antenna.

The receiver is the inverse of this process. The signal from the antenna passes through the band pass filter, which is in this case acting as a pre-selection filter. The received signal passes through the integrated LNA and is converted to an IF of 374MHz. The signal then passes through a SAW filter, which acts to reject adjacent channels as defined by the 802.11 standard. Due to the bandwidth of this filter, adjacent channels must be at least 20MHz apart. The filtered IF signal is then down-converted to baseband I and Q components.

The local oscillators required by the mixing process are generated by internal IF and RF PLL frequency synthesizers. These are controlled through a three-wire serial data interface.

GENERAL APPLICATION INFORMATION

This part is used at high frequencies. Proper attention to layout and component selection is critical in order to achieve the specified performance. Values for DC blocking capacitors and power supply bypass capacitors should be selected so that they are series self-resonant at the frequency of operation. In addition, transmission line techniques should always be used on signal lines at RF frequencies, and may be required on signal lines at IF frequencies if connections are long with respect to wavelength.

The RF9008 should be powered from regulated supply. If not sharing this supply with the MCLK oscillator, the MCLK oscillator should also be powered from a well-regulated supply. Avoid sharing the RF9008 and MCLK oscillator supplies with the baseband processor and/or MAC. Failure to provide proper decoupling will result in high EVM and spectral masks compliance at lower output powers.

Power supply bypassing of VCC lines for the PLL is critical in order to minimize the effects of power supply noise on phase noise performance. In addition to RF/IF bypassing, these lines should be bypassed with low-frequency capacitors. A value of 0.01μF is sufficient for most applications, but performance should be verified by looking at a modulated signal on a vector signal analyzer or a constant signal on a spectrum analyzer or phase noise test set.

Since this is a mixed-signal device, care should be taken to separate traces connecting to digital circuits from those connecting to analog circuits. Power supply bypassing is important to keep the noise contributions of digital circuits to a minimum. It is generally better to start with more bypassing than you think you need, then remove components and re-evaluate performance.

ENABLE/DISABLE MODES

Operation of the device is controlled by the MODE0 and MODE1 pins according to the following truth table.

MODE0	MODE1	Function
0	0	Idle
0	1	Transmit Enable
1	0	Receive Enable
1	1	Reset

When switching between modes, ensure that MODE0 and MODE1 are high for less than three master clock cycles to avoid inadvertently entering reset modes. To enter reset mode, ensure that MODE0 and MODE1 are high for at least five master clock cycles.

When in Idle mode, the IF and RF PLLs are locked and the baseband circuitry is powered; everything else is disabled. In Reset mode, the voltage regulators for the digital circuitry inside the part are enabled; everything else is disabled.

Additionally, there is a hibernate mode in which everything is disabled. This mode is entered by writing the value 8h to Register 0 while in hibernate mode. The MODE0 and MODE1 pins should be held high while in hibernate mode. To exit this mode, toggle the states of one or both MODE pins. All registers will need to be reprogrammed on exiting hibernate mode.

RECEIVER

Front End LNA/Mixer

The LNA/Mixer provides 35dB conversion gain to IF in high-gain mode to detect weak signals at the antenna. In low-gain mode, the LNA/Mixer provides 2dB conversion gain. The LNA GS pin selects gain mode. When LNA GS is high, the part is in high-gain mode. The mixer output is connected to the IF OUT pins as a differential signal for connecting to an external SAW filter. Proper matching at the input and output of the SAW filter is essential for maintaining performance through the system. The IF input and output differential impedances are 750Ω nominal. The same filter is used for transmitter and receiver. Internal switches control which signal is present at the SAW filter.

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IF/Baseband

The filtered IF signal is processed through a variable gain amplifier controlled through the RX VGC pin. The IF signal is then downconverted to baseband I and Q signals, which are then filtered on-chip with third order Bessel filters. The IF-to-baseband conversion gain range is 4dB to 72dB depending on the voltage present on the RX VGC pin. The gain slope is negative over a range of 1.2V to 2.0V.

The single-ended I and Q outputs should be DC-coupled to the baseband processor. The DC reference voltage should be provided to the baseband processor through the VREF pin to eliminate the potential for a signal blocker at DC.

TRANSMITTER

The I and Q inputs are differential. To use single-ended inputs, place 0.01μF capacitors at the I BYP and Q BYP pins. The inputs should be DC-coupled from the baseband processor. In order to improve carrier suppression at RF, the DC reference voltage should be provided to the baseband processor through the VREF pin. The baseband input signals are filtered on-chip using third order Bessel filters for spectral shaping. The signals are then complex upconverted to IF. The IF mixer output is amplified and connected to the IF OUT pins as a differential signal for connecting to the external SAW filter as described above.

The differential signal from the SAW filter is then amplified using a variable gain amplifier. The gain of this amplifier can be controlled either through the analog TX VGC pin or digitally from the baseband processor or MAC, depending on application. The signal is then upconverted to the desired RF output frequency and amplified to a level appropriate to drive a PA to the desired output level at the antenna.

DUAL FREQUENCY SYNTHESIZER

IF LO PLL

The IF PLL is an integer-N PLL nominally programmed to a center frequency of 748MHz. This frequency is divided by two at the IF converter. A 22MHz or 44MHz oscillator is required to provide the PLL reference frequency through the MCLK pin. See the Register Details and Serial Data Interface sections for details on programming.

RF LO PLL

The RF LO PLL is a fractional-N PLL programmed to an appropriate frequency to convert the 374MHz IF to the desired RF channel. The nominal step size is 22MHz with a fractional modulus of 2^{24}. The 22MHz or 44MHz reference frequency is divided to the appropriate step size. See the Register Details and Serial Data Interface sections for details on programming.

Note: To ensure proper operation of the PLLs, program Register 12 [17:16] to ‘11b’. All other bits in Register 12 should be set to ‘0’.

PLL Calibration

The purpose of the calibration is to select the correct V_{CO} band for the chosen RF channel and adjust the charge pump current (KV_{CAL}) to normalize the varactor response. Both RF and IF PLL synthesizers go through a calibration routine whenever the 9008 comes out of Sleep or Reset modes (MODE 0 or MODE 1 go to ‘0’) or when the RF channel is changed. It will also be initiated automatically if AUTOCAL_EN (IF or RFPLL1 <10>) and LD_EN (IF or RFPLL1 <9>) are both set to ‘1’ and the PLL goes out of lock.

The completion of a calibration cycle is indicated in a Register 31 (address 0x1F that can be accessed by the host processor. The Test Register (address 0x1B) is used to direct the specific PLL registers to Register 31 according to Test Register <12:11> settings (‘01’ RF PLL information or ‘10’ IF PLL information). It is recommended to read the Test Register and can only bits 12 and 11. Calibration is complete and the PLL’s are locked when Register 31 (address 0x1F, bits <17:16>)=‘10’.

To measure the calibration and lock time from a mode change, the recommended procedure for the MAC is:
1. Set the RF9008 in IDLE mode (MODE 0 and MODE 1="00").
2. Program the desired information, including RF channel and TEST register.
3. Reset the RF9008 for a minimum of 3 MCLK Cycles (MODE 0 and MODE 1="11").
4. When ready, clear either or both MODE 0 and MODE 1 to initiate the change from RESET mode. Start timer on change.
5. Start polling register 31, testing bits <17:16> and repeat polling until the bits <17:16> read '10'. Stop timer and calculate and lock calibration time.

To measure from a channel frequency change, the recommended procedure for the MAC is:
1. Set the RF9008 in IDLE mode (MODE 0 and MODE 1="00").
2. Program the desired information, including RF channel (1 or 14) and TEST register.
3. Program new channel (14 or 1) making note to start timer when SSB returns to '1' after final programming of synthesizers.
4. Start polling register 31, testing bits <17:16> and repeat polling until the bits <17:16> read '10'. Stop timer and calculate and lock calibration time.

SERIAL DATA INTERFACE

A three wire serial data interface allows user programming of the internal control registers in the RF9008. The serial data interface consists of the serial select (SSB), serial data in (SDI) and serial clock (SCLK) pins. The SDI is a bi-directional pin, by default it is configured as an input to the serial interface, but during a read session it is used as an output.

The first bit in a serial transfer (the MSB) is the read/write (R/W) bit. R/W=1 for a read, and R/W=0 for a write. After each register read, the chip select (SSB) must go high for one MCLK cycle to reset the SDI pin to input condition before the next operation.

The figure below shows a timing diagram for a serial transfer to the RF9008 serial data interface. The serial select (SSB) pin is normally high. A serial transfer is initiated by taking SSB low. The address and data bits on the serial data in (SDI) pin are shifted in on rising edges of the serial clock (SCLK) pin, MSB first. The data is latched and changes take effect on the falling edge of the clock pulse corresponding to the last (18^{th}) data bit in the addressed register. If the transfer is interrupted, such that the 18^{th} data bit clock pulse does not occur, then no data is written to the register.

When the synthesizers are programmed, an internal pulse is generated alerting the synthesizer that a new setting is required. In order to guarantee that this internal pulse is long enough, the time between the falling edge of the last serial clock pulse and the rising edge of SSB must be at least 1/fr.

The RF9008 can be reset to its power on condition (including register defaults) by writing '011111b' plus 18 don't care bits to the serial data interface. The reset is actually performed when the SSB is raised after the write. Although this command can be performed during any settings of the MODE0 and MODE1 pins, care should be taken to ensure that the registers are reprogrammed in a sufficient time to perform any transmit or receive operations.

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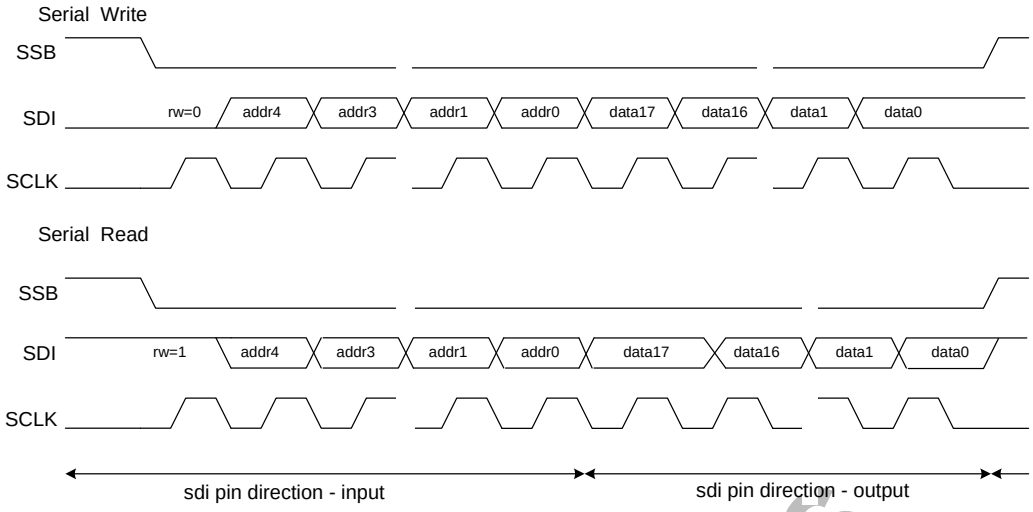

REGISTER DETAILS

The individual registers and bits are described below. A write instruction to address 11111 causes global reset. All programming values are binary unless otherwise specified.

Configuration Register 1 (CFG1)-Address 00000

Location	Bit Name	Default	
CFG1(17:16)	reserved	00	Reserved, program to zero (0)
CFG1(15:14)	REF_SEL(1:0)	00	Reference Divider Value 0 0 Divide by 2 1/2 high, 1/2 low 0 1 Divide by 3 1/3 high, 2/3 low 1 0 Divide by 44 1/44 high, 43/44 low 1 1 Divide by 1 (bypass)
CFG1(3)	HYBERNATE	0	Sleep Mode Current 0=nominal sleep mode current 1=very low sleep mode current
CFG1(2)	RF_VCO_ REG_EN	1	RF VCO Regulator Enable 0=disabled 1=enabled
CFG1(1)	IF_VCO_ REG_EN	1	IF VCO Regulator Enable 0=disabled 1=enabled
CFG1(0)	IF_VGA_ REG_EN	1	IF VGA Regulator Enable 0=disabled 1=enabled

IF PLL Register 1 (IFPLL1)-Address 00001

Location	Bit Name	Default	
IFPLL1(17)	PLL_EN1	0	IF PLL Enable 0=disabled 1=enabled
IFPLL1(16)	KV_EN1	0	IF PLL KV Calibration Enable 0=disabled 1=enabled
IFPLL1(15)	VTC_EN1	1	IF PLL Coarse Tune Enable 0=VCO coarse tuning system is disabled 1=VCO coarse tuning system is enabled
IFPLL1(14)	LPF1	0	IF PLL Loop Filter Bypass 0=Internal loop filter is used 1=Internal loop filter is bypassed and External loop filter is used
IFPLL1(13)	CPL1	0	IF PLL Charge Pump Leakage Current 0=minimum value 1=2xminimum value
IFPLL1(12)	PDP1	1	IF PLL Phase Detector Polarity 0=positive, VCO frequency increases with increasing tuning voltage 1=negative, VCO frequency decreases with increasing tuning voltage
IFPLL1(11)	AUTOCAL_ EN1	0	IF PLL Auto Calibration Enable 0=disabled 1=enabled
IFPLL1(10)	LD_EN1	0	IF PLL Lock Detect Enable 0=disabled 1=enabled
IFPLL1(9)	P1	0	IF PLL Prescaler Modulus 0=4/5 Mode 1=8/9 Mode
IFPLL1(8:4)	Reserved	00000	Reserved, program to zero (0)

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IFPLL1(3:0)	DAC1(3:0)	3h	IF VCO Coarse Tuning Voltage LPF_V1=int (coarse tuning voltage/V_{DD})x16

IF PLL Register 2 (IFPLL2)-Address 00010

Location	Bit Name	Default	
IFPLL2(17:16)	Reserved	0	Reserved, program to zero (0)
IFPLL2(15:0)	IF_N(15:0)	22h	IFPLL divide-by-N value

IF PLL Register 3 (IFPLL3)-Address 00011

Location	Bit Name	Default	
IFPLL3(17)	Reserved	0	Reserved, program to zero (0)
IFPLL3(16:8)	DN1(16:8)	1FFh	IF VCO KV Calibration, delta N value (signed 2's complement) DeltaF=DN1/(Fr)
IFPLL3(7:4)	CT_DEF1(3:0)	7h	IF VCO Coarse Tuning Value
IFPLL3(3:0)	KV_DEF1(3:0)	8h	IF VCO KV Calibration, default value

RF PLL Register 4 (RFPLL1)-Address 00100

Location	Bit Name	Default	
RFPLL1(17)	PLL_EN	0	RF PLL Enable 0=disabled 1=enabled
RFPLL1(16)	KV_EN	0	RF PLL KV Calibration Enable 0=disabled 1=enabled
RFPLL1(15)	VTC_EN	1	RF PLL Coarse Tune Enable 0=VCO coarse tuning system is disabled 1=VCO coarse tuning system is enabled
RFPLL1(14)	LPF	0	RF PLL Loop Filter Bypass 0=Internal loop filter is used 1=Internal loop filter is bypassed and External loop filter is used
RFPLL1(13)	CPL	0	RF PLL Charge Pump Leakage Current 0=minimum value 1=2xminimum value
RFPLL1(12)	PDP	1	RF PLL Phase Detector Polarity 0=positive, VCO frequency increases with increasing tuning voltage 1=negative, VCO frequency decreases with increasing tuning voltage
RFPLL1(11)	AUTOCAL_EN	0	RF PLL Auto Calibration Enable 0=disabled 1=enabled
RFPLL1(10)	LD_EN	0	RF PLL Lock Detect Enable 0=disabled 1=enabled
RFPLL1(9)	P	0	RF PLL Prescaler Modulus 0=8/9 Mode 1=8/10 Mode
RFPLL1(8:4)	Reserved	00000	Reserved, program to zero (0)

RFPLL1(3:0)	DAC(3:0)	3h	RF VCO Coarse Tuning Voltage LPF_V1=int (coarse tuning voltage/V_{DD})x16

RF PLL Register 5 (RFPLL2)-Address 00101

Location	Bit Name	Default	
RFPLL2(17:6)	N2(11:0)	5Eh	RF PLL Divide By N Value
RFPLL2(5:0)	NUM2(23:18)	0	RF PLL Numerator Value

RF PLL Register 6 (RFPLL3)-Address 00110

Location	Bit Name	Default	
RFPLL3(17:0)	NUM2(17:0)	0	RF PLL Numerator Value

Note: Registers 5 and 6 must be written while in reset mode.

RF PLL Register 7 (RFPLL4)-Address 00111

Location	Bit Name	Default	
RFPLL4(17)	Reserved	0	Reserved, program to zero (0)
RFPLL4(16:8)	DN(8:0)	145 h	RF VCO KV Calibration, delta N value (signed 2's complement) DN=(deltaF/Fr)*256
RFPLL4(7:4)	CT_DEF(3:0)	7h	RF VCO Coarse Tuning Value
RFPLL4(3:0)	KV_DEF(3:0)	8h	RF VCO KV Calibration, default value

Calibration Register 8 (CAL1)-Address 01000

Location	Bit Name	Default	
CAL1(17:13)	TVCO(4:0)	0Fh	VCO1 Warm-up Time TVCO1=(approximate warm-up time)x(Fr/32)
CAL1(12:8)	TLOCK(4:0)	07h	VCO1 Tuning Gain Calibration, approximate lock time TLOCK1=(approximate lock time)x(Fr/128)
CAL1(7:3)	M_CT_VALUE (4:0)	08h	VCO1 Coarse Tune Calibration Reference clock averaging time M_CT_VALUE=(averaging time)x(Fr/32)
CAL1(2:0)	LD_WINDOW (2:0)	2h	Lock Detect Resolution 0 through 7

TXRX Register 9 (TXRX1)-Address 01001

Location	Bit Name	Default	
TXRX1(17)	RXDCFBBYPS	0	Receiver DC Removal Loop 0=Enable DC Removal Loop 1=Disable DC Removal Loop
TXRX1(16:15)	PCONTROL (1:0)	00	00 External TXVGC Controls VGA 01 External TXVGC Controls VGA 10 Internal Control of VGA from Register TXVGC(4:0) 11 Internal Control of VGA from Power Control
TXRX1(14:10)	TXVGC(4:0)	00000	Transmit Variable Gain Select 0h-1Fh High gain to low gain

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TXRX1(9:7)	RXLPFBW (2:0)	010	Receive Baseband Low Pass Filter Bandwidth Selection 000=Wide Bandwidth 111=Narrow Bandwidth
TXRX1(6:4)	TXLPFBW (2:0)	010	Transmit Baseband Low Pass Filter Bandwidth Selection 000=Wide Bandwidth 111=Narrow Bandwidth
TXRX1(3)	TXDIFFMODE	0	Switches Between Single-Ended and Differential Mode 0=Single-ended mode 1=Differential mode
TXRX1(2)	TXENMODE	0	Input Buffer Enable TX 0=Input Buffer Controlled by TXEN 1=Input Buffer Controlled by BBEN
TXRX1(1)	INTBIASEN	0	Internal Bias Enable 0=Disabled - External Bias Required 1=Enabled - Internal Bias Enabled
TXRX1(0)	TXBYPASS	0	TX Baseband Filters Bypass 0=Not Bypassed 1=Bypassed

Power Control Register 10 (PCNT1)-Address 01010

Location	Bit Name	Default	
PCNT1(17:15)	MID_BIAS(2:0)	000	Used to setup the voltage provided by the PA_BIAS AMPLIFIER to determine the BIAS VOLTAGE to provide to the PA when the desired output power is MID_POWER. The MID_BIAS selection will select a V_{OUT} on PBIAS between 1.6V and 2.6V.
PCNT1(14:9)	P_DESIRED (5:0)	000000	User selectable desired output power at antenna. The 5 MSB's are integer portion in dBm. The LSB is 0.5dBm. Example: +19.5dBm is represented by 100111.
PCNT1(8:3)	PC_OFFSET (5:0)	000000	User programmable offset to adjust to process/board variations in the power control loop. This is a 2's-complement value with the LSB equal to 0.5dB.
PCNT1(2:0)	TX_DELAY (2:0)	000	User programmable delay to allow a single TX_PE line to be used to enable the BBP and the radio function. Programmable in 0.5us increments from 0us to 3.5us.

Power Control Register 11 (PCNT2)-Address 01011

Location	Bit Name	Default	
PCNT2(17:12)	MAX_POWER (5:0)	000000	User programmable MAX output power provided when PABIAS=2.6V. This allows the power control function to be customized for various PA's. The 5 MSB's are integer portion in dBm. The LSB is 0.5dBm.
PCNT2(11:6)	MID_POWER (5:0)	000000	User programmable MAX output power provided when PABIAS=MID_BIAS. This allows the power control function to be customized for various PA's. The 5 MSB's are integer portion in dBm. The LSB is 0.5dBm.
PCNT2(5:0)	MIN_POWER (5:0)	000000	User programmable MAX output power provided when PABIAS=1.6V. This allows the power control function to be customized for various PA's. The 5 MSB's are integer portion in dBm. The LSB is 0.5dBm.

VCOT1 Register 1 (VCOT1)-Address 01100

Location	Bit Name	Default	
VCOT1(17)	AUX	0	IF VCO Band Current Compensation 0=disabled 1=enabled
VCOT1(16)	AUX1	0	RF VCO Band Current Compensation 0=disabled 1=enabled
VCOT1(15:0)	Reserved	0	Reserved, program to zero (0)

Test Register 1 (TEST)-Address 11011

This is a test register for internal use only.

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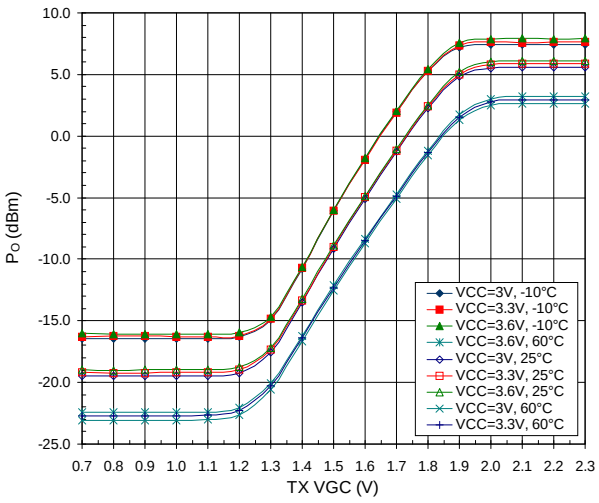
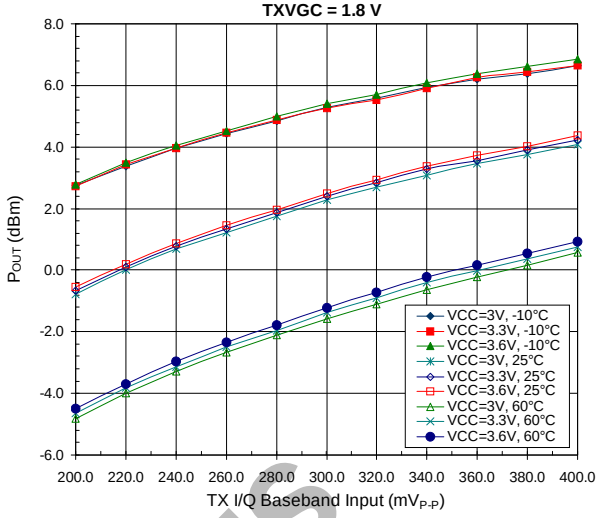
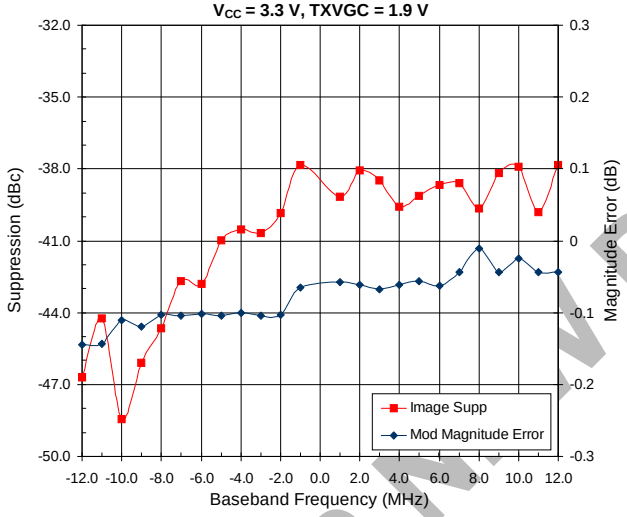
P_{OUT} (CW) versus TX VGC



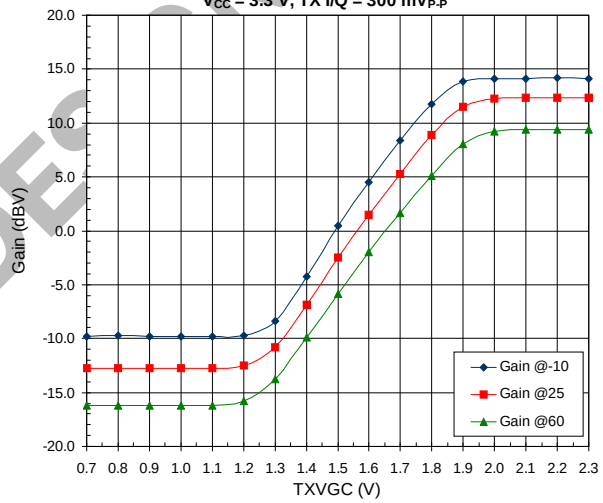
P_{OUT} (CW) versus TX I/Q Input
TXVGC = 1.8 V



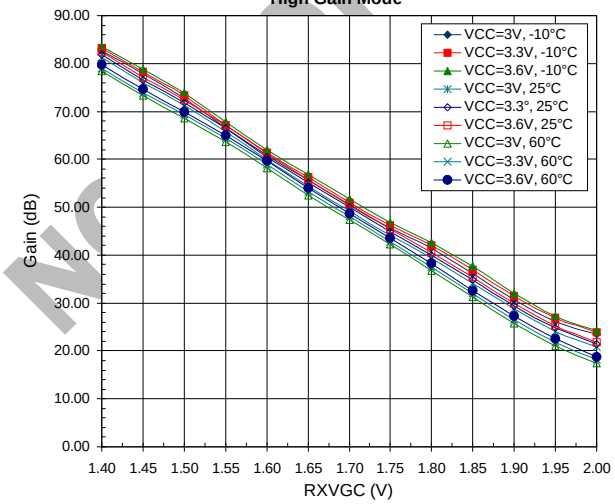
Modulation Magnitude Error and Image Suppression
V_{CC} = 3.3 V, TXVGC = 1.9 V



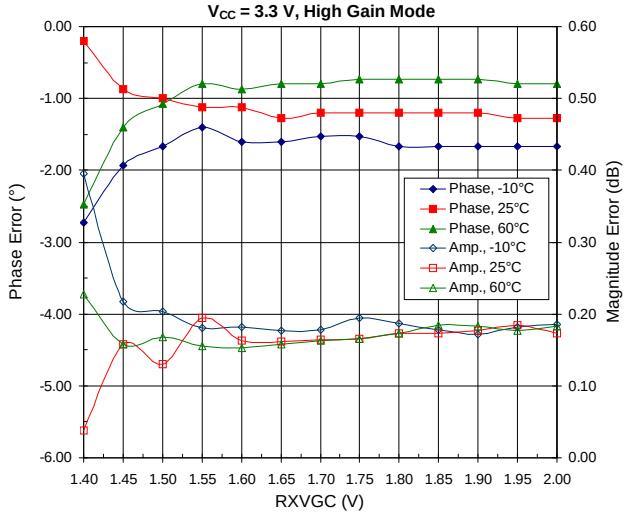
TX Gain versus TXVGC, Temperature
V_{CC} = 3.3 V, TX I/Q = 300 mV_{P-P}

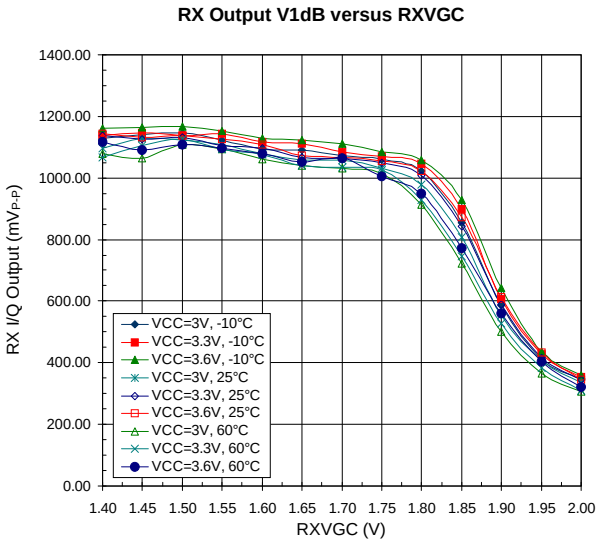


RX Gain versus RXVGC
High Gain Mode



RX Magnitude and Phase Error versus RXVGC
V_{CC} = 3.3 V, High Gain Mode





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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is Electroless Nickel, immersion Gold. Typical thickness is 3μinch to 8μinch Gold over 180μinch Nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

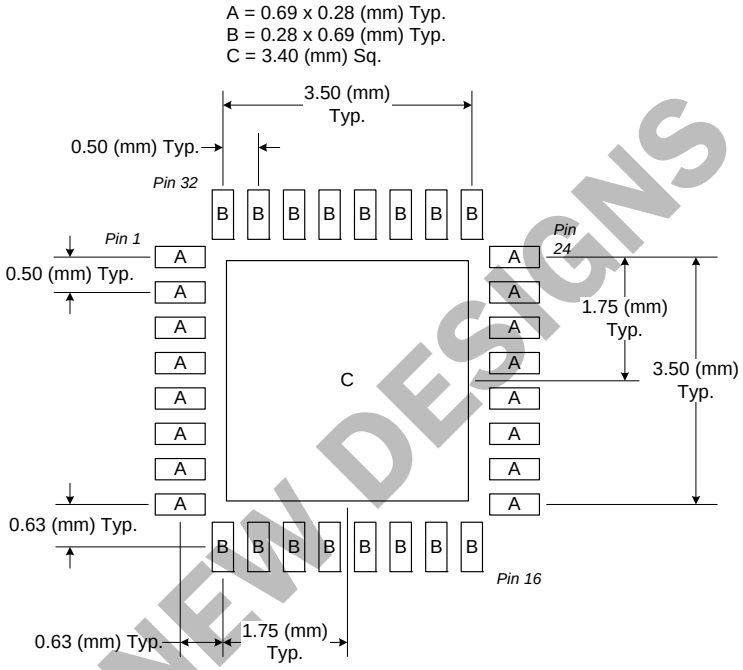

Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

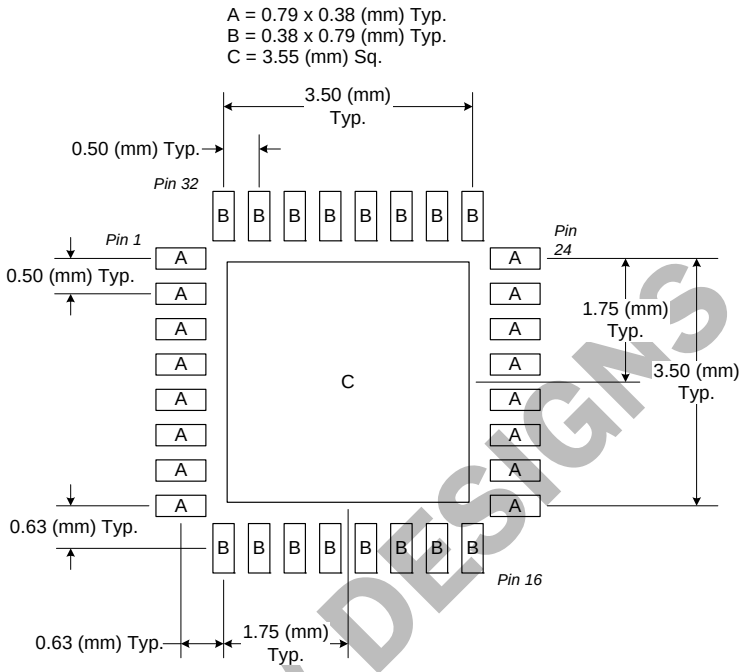

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB Metal Land Pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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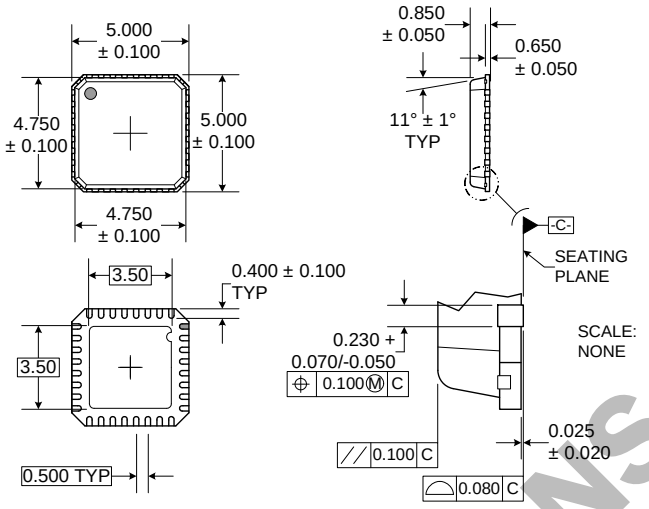
Package Drawing
QFN, 32-Pin, 5x5 (Supplier 2)



Dimensions in mm.
Shaded area indicates pin 1.

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